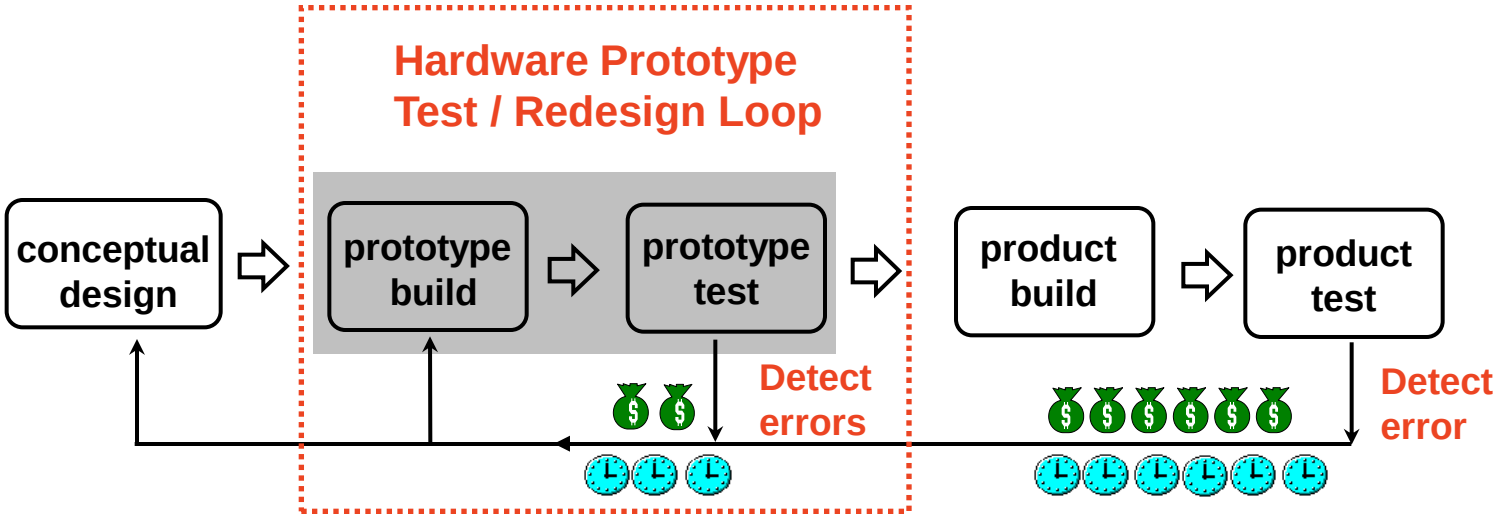
Virtual Prototyping of Power Supply Designs

Using Design Verification Module (DVM) To Reduce Design Cycle Time

April 21, 2011
You-Shang Technical Corp. Seminar
Thomas G. Wilson, Jr.
SIMPLIS Technologies

Hardware-Focused Product Development Procedure



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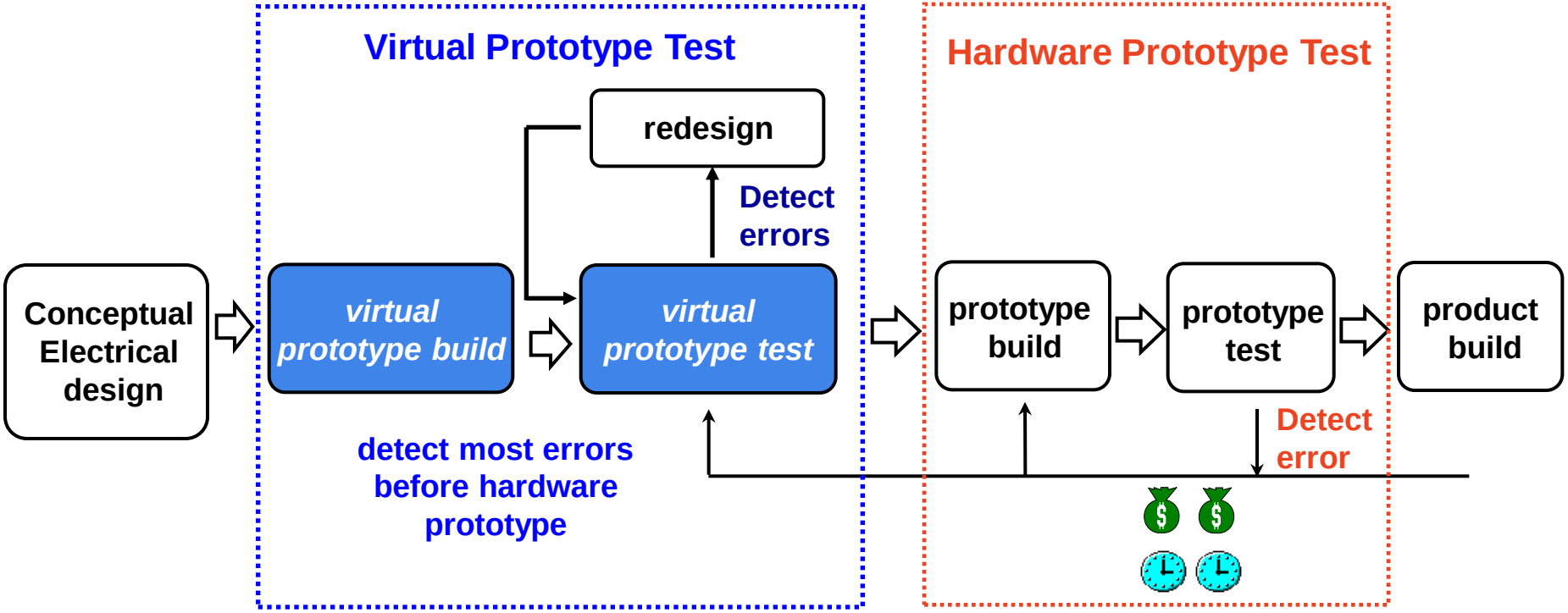
Development Process with Virtual Prototype emphasis



Over 50% of all electrical design errors
can be detected by Virtual Prototyping Process
No other single design improvement can achieve more than 2% design error reduction

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Virtual Prototyping of Power Supply Designs

- Cost of Design Changes increasing
  - Design Changes delay time to profitable manufacture
  - All Design Changes consume valuable New Product delivery capacity
- Cost of Hardware Iterations increasing
  - Time to market requirements are shrinking
  - As size of power supplies shrink, $$ cost of additional hardware iterations increases
- Cost of correcting Design Errors increases dramatically the later they are discovered in the process

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Power Supply Electrical Design Errors

- The following data is the result of in-depth studies of five large design organizations at three major manufacturers of custom and standard power supplies.
- All engineering change orders during the study period (6 to 9 months) were evaluated to determine the nature of the change, whether or not it resulted in a PCB spin, and whether or not it could have been detected with simulation.

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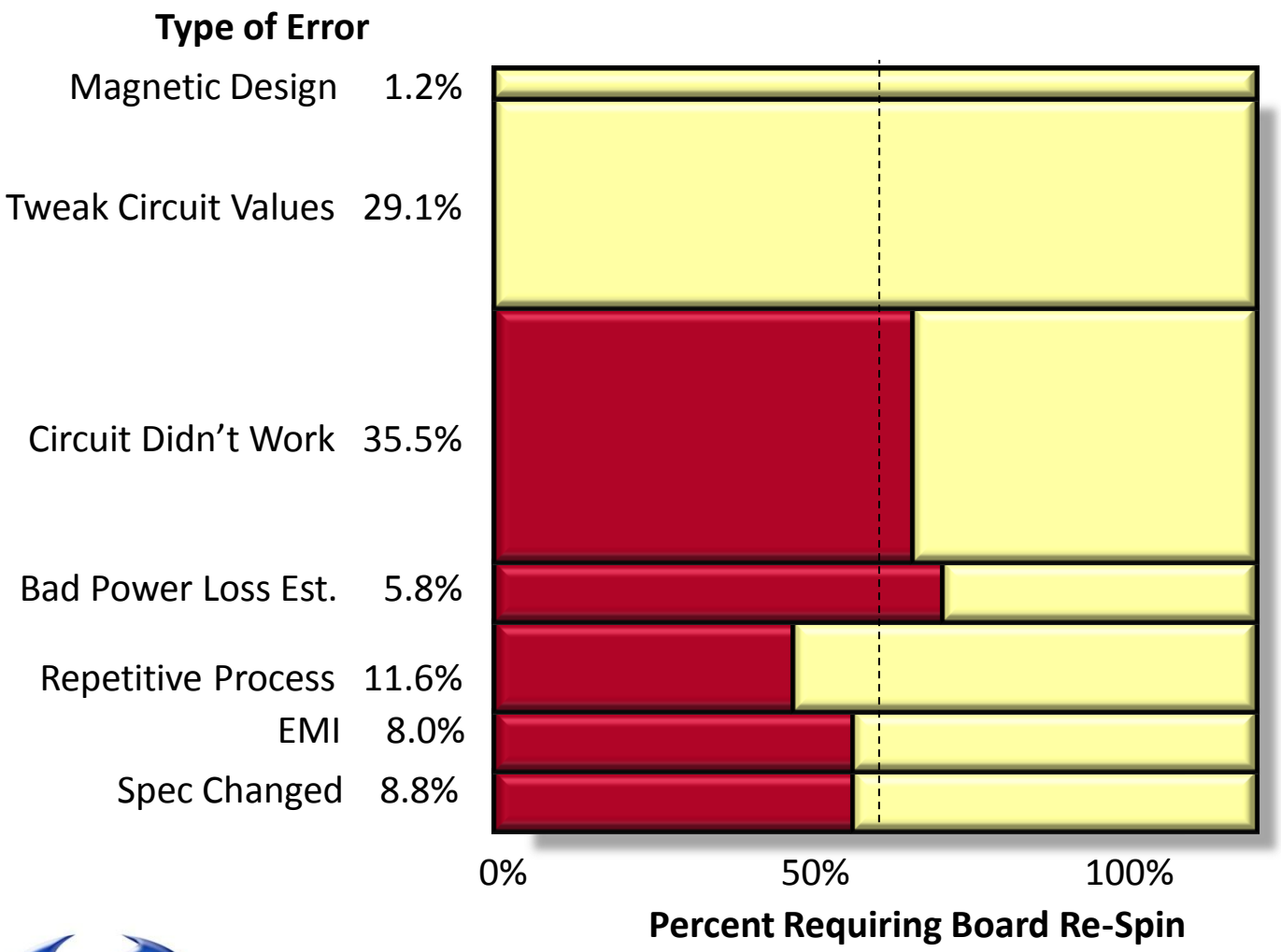
Survey of PS Electrical Design Errors



34% of all design errors in the study required a new PCB spin.

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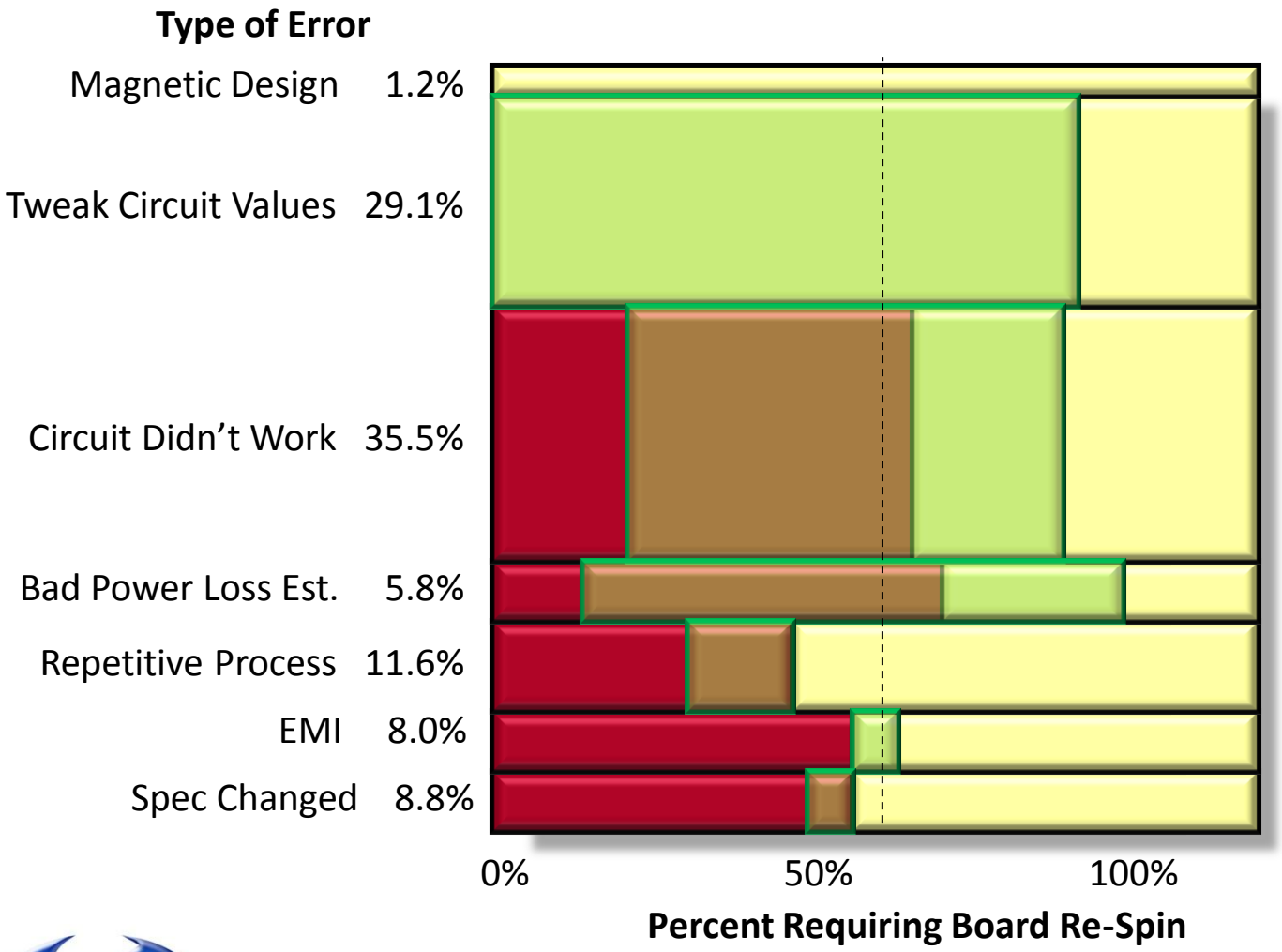
Errors Detectable by Simulation



SIMPLIS could detect 51% of all errors and 56% of errors that required a board spin.

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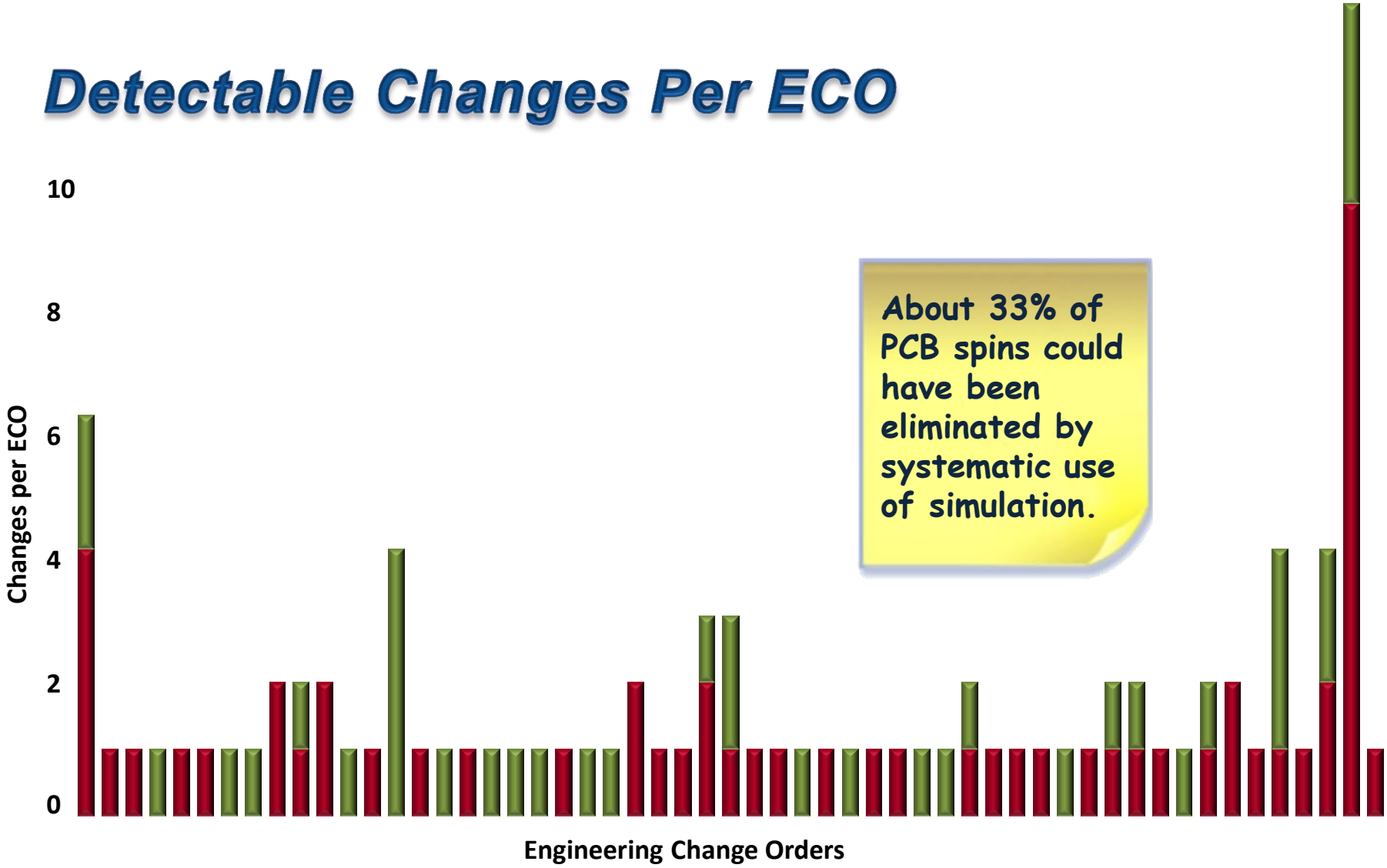
Detectable Changes Per ECO



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Virtual Prototyping of Power Supply Designs

- Virtual Prototyping Objective
  - Reduce number of latent design errors that are left to be discovered in prototype hardware
    - Reduce number of hardware iterations required to meet design requirements
      - Reduce time before design can be profitably manufactured
  - **Get design into profitable manufacture as soon as possible**

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Virtual Prototyping of Power Supply Designs

Virtual Prototypes will not replace Hardware Prototypes any time soon, so why bother?

- Benefits of reducing hardware iterations
  - Reduce time to profitable design
  - Reduce development cost
  - Increase effective development capacity
- No other single process improvement comes within an order of magnitude of this level of benefit

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Virtual Prototyping – why now?

- Costs of failure rising sharply
  - NT$$
  - Time
- Costs of simulation have fallen
  - NT$$
  - Time
    - ***Time to valuable simulation results has fallen below critical threshold in many applications***

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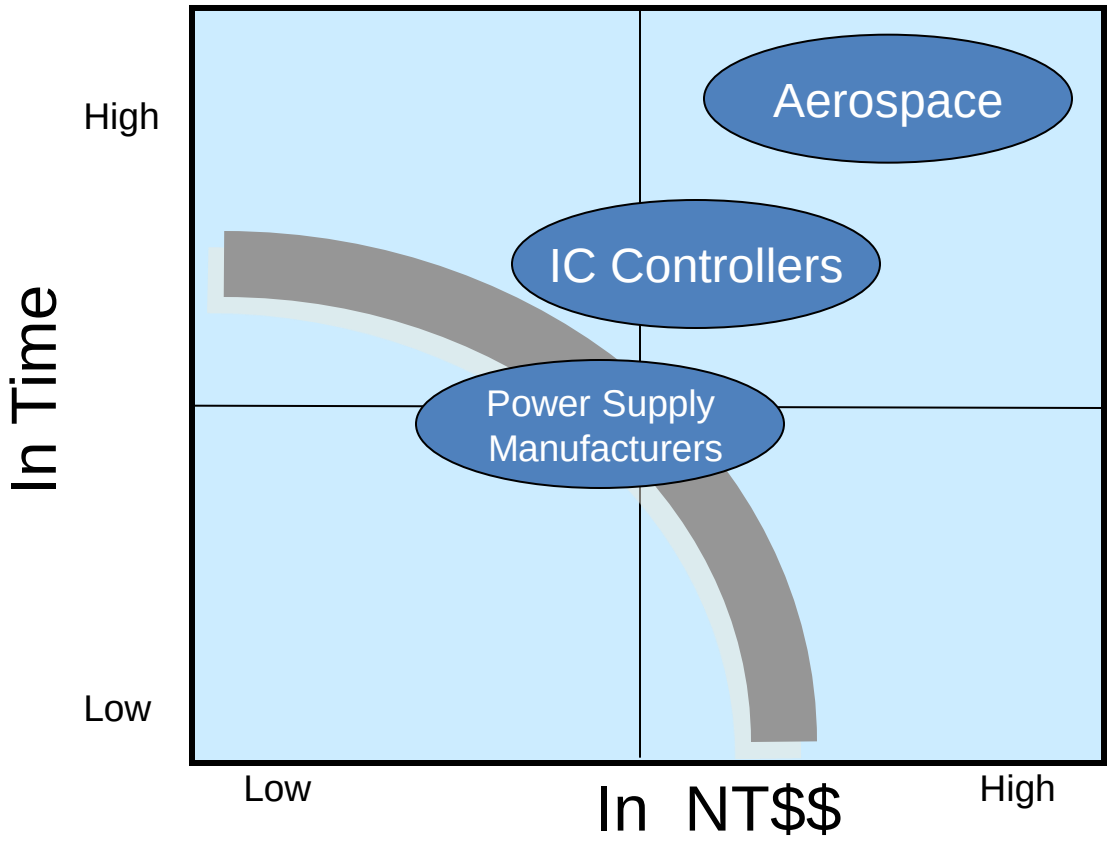
D14.1 - D14.4

Pain Threshold – when does Virtual Prototyping make sense?

Cost of Failure / Cost of sim results



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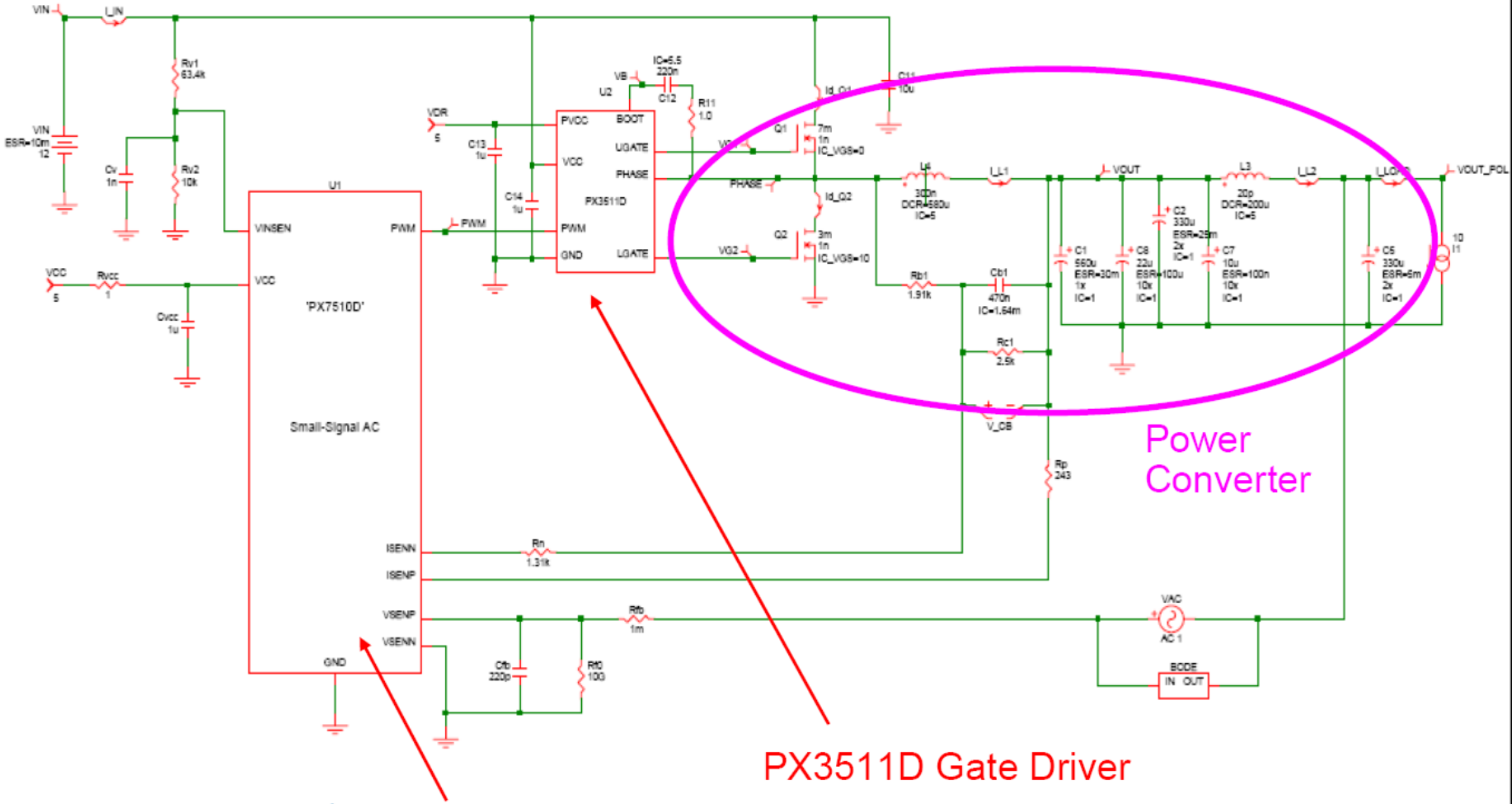
Time-Domain Simulation Model

SIMPLIS Simulation Circuit & IC Model

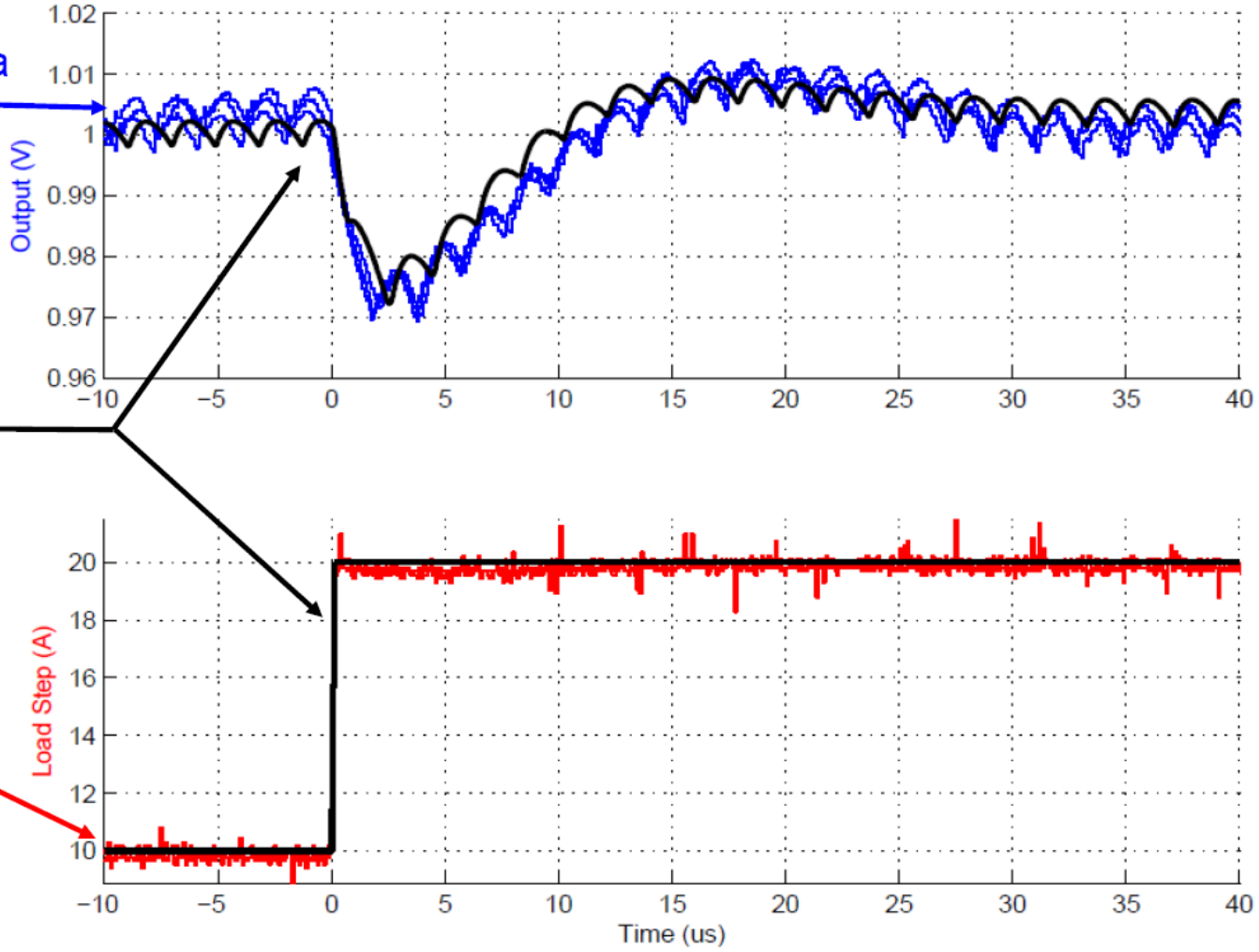


Time-Domain Simulation vs. Experimental Results

Output Voltage
Imported Scope Data
3 Traces

SIMPLIS™
Simulation Model

10 A to 20 A
Load Step
A 10 A Step
with a 10 A
Static Load



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Infineon Digital Power

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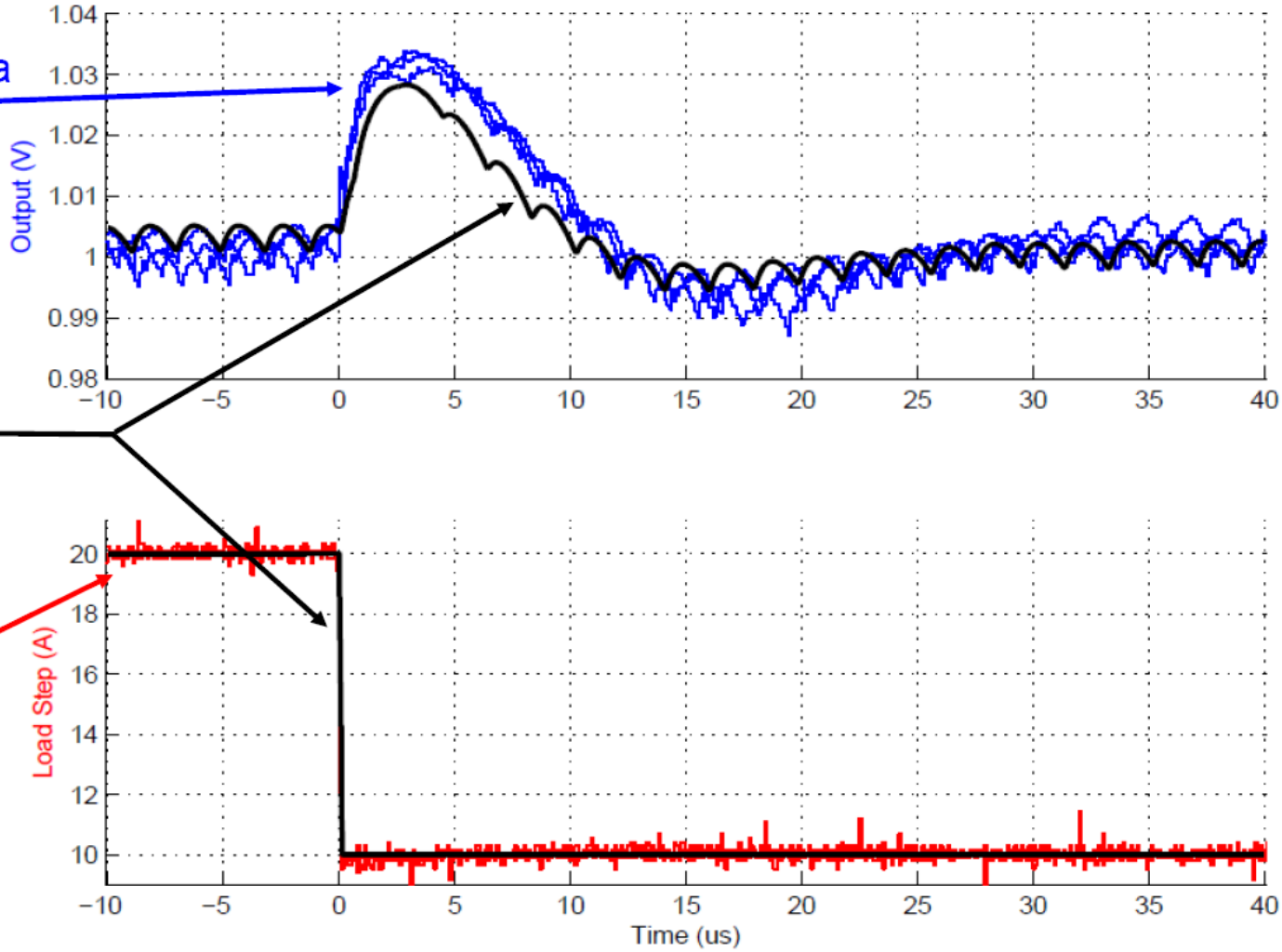

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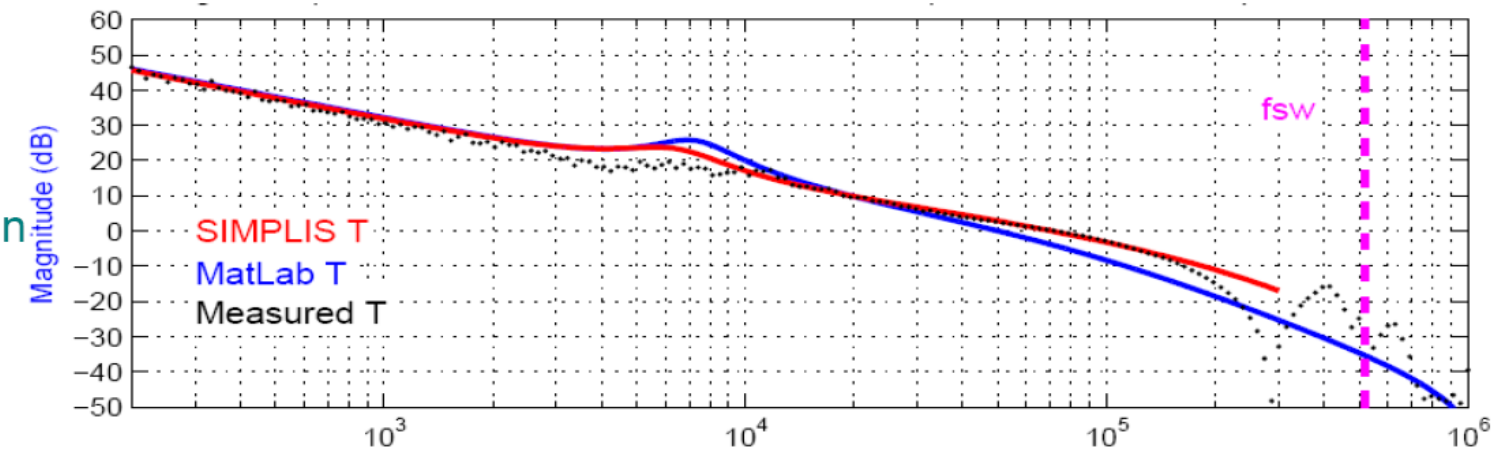
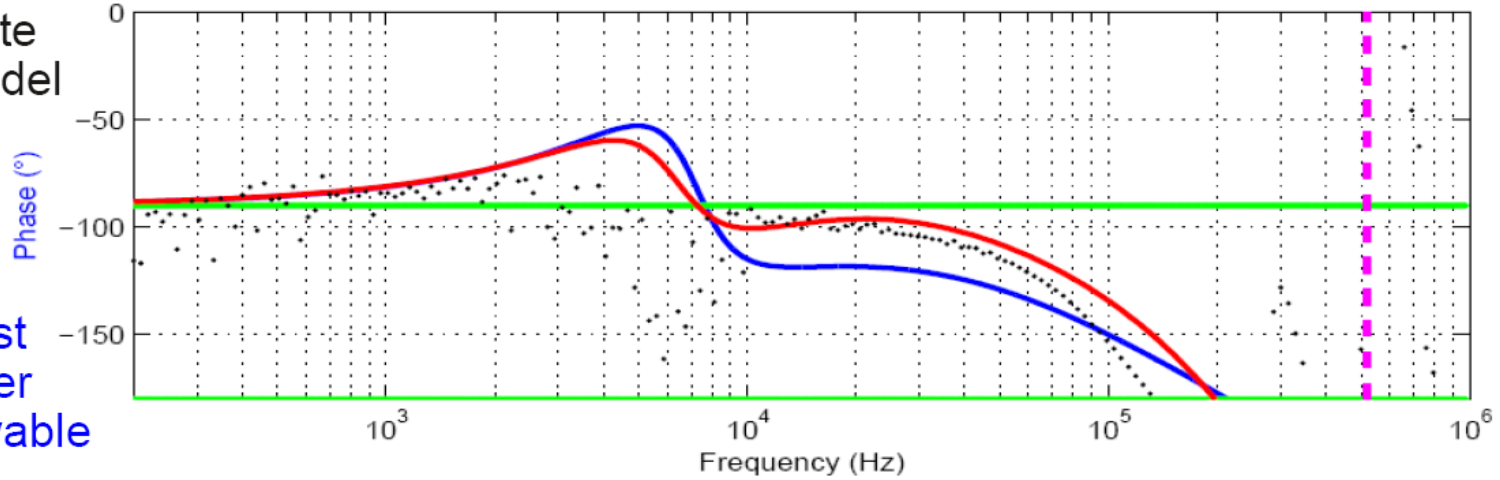
Frequency-Domain Comparison: Complex Zeroes

This is a more aggressive design



The MatLab model shown here uses a more accurate digital loop model



More phase boost throughout, higher crossover achievable

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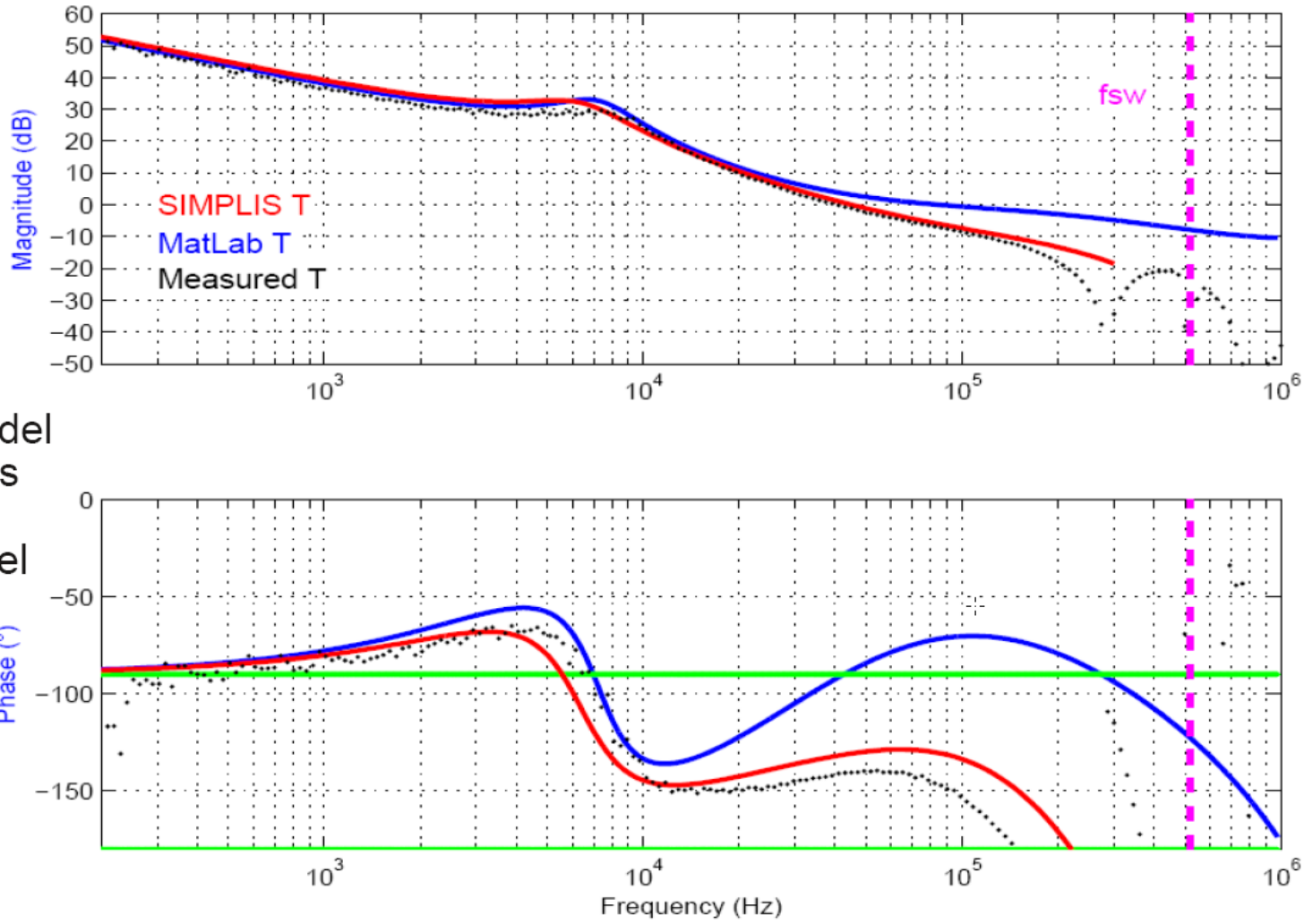
Frequency-Domain Comparison: Real Zeroes



The MatLab model shown here uses a simplified digital loop model

Both the gain and phase are less accurate at the higher frequencies

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SIMPLIS Virtual Prototyping capability

- SIMPLIS gives very accurate results for closed loop behavior
- How about stress and loss analysis?
  - What is needed to get good power loss estimates?
    - Given that switching loss measurements are more challenging than measuring loop response behavior

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Switching Losses

- Switching losses are very sensitive to
  - Device parasitic elements
  - Layout parasitic elements
- Device parasitics can be characterized in advance
- For maximum benefit, virtual prototyping is done ***before*** a layout exists
  - So there are inherent uncertainties in this effort
- This area of simulation is less mature than simulation of closed loop performance
- Even so, *the initial estimate of switching losses plays a central role in the development process*

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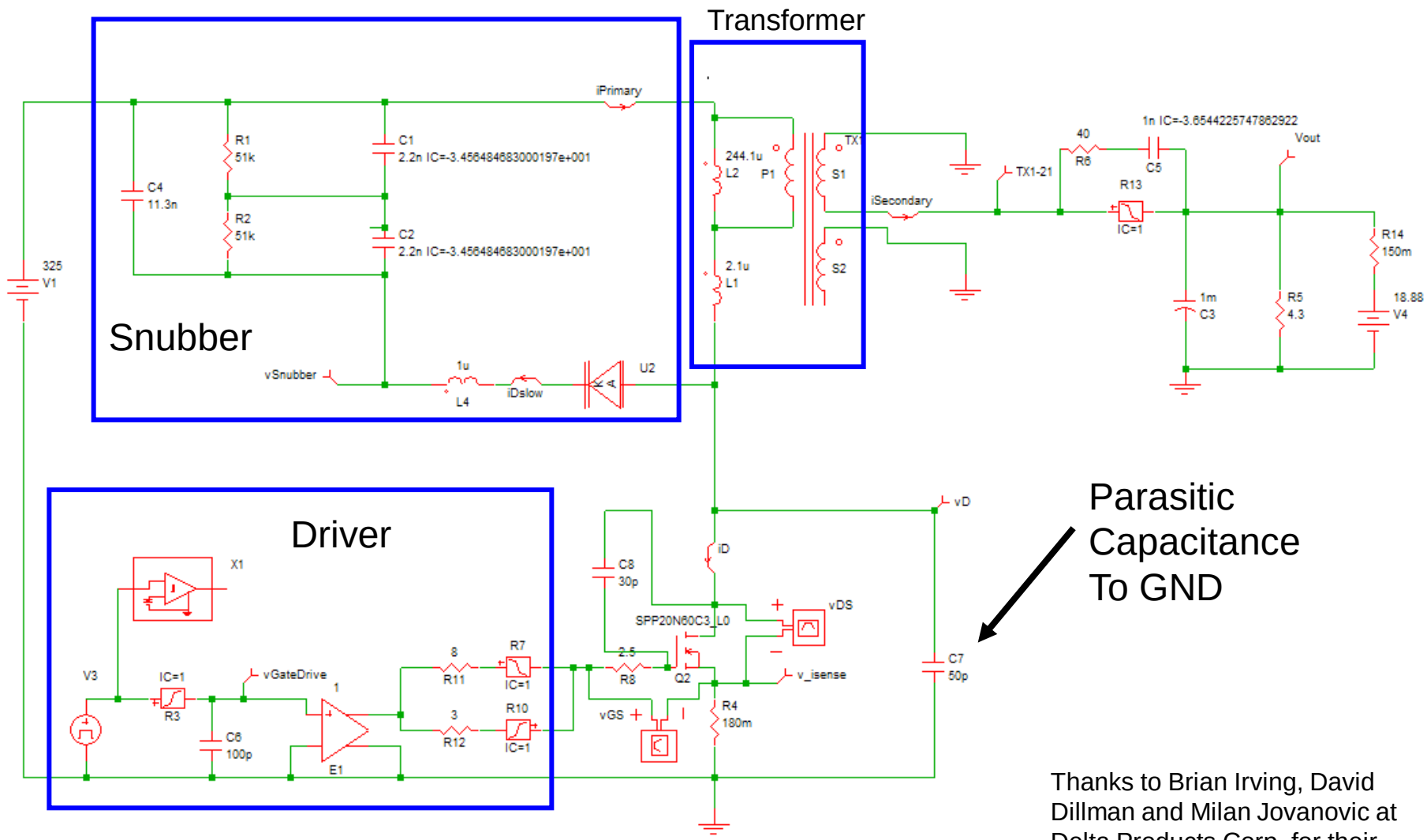
Switching Losses – Flyback for Adapter



Parasitic Capacitance To GND

Thanks to Brian Irving, David Dillman and Milan Jovanovic at Delta Products Corp. for their support in this effort

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Switching Losses – Flyback for Adapter

- Run simulation test circuit open loop in Steady State
- Adjust Driver, FET and Snubber Diode models to match measured waveforms at Vin = 325V, Vout = 18.88V and Full Load Iout = 4.74A
- Then compare simulated waveforms and measured waveforms at different line and load conditions with “identical” gate drive signals

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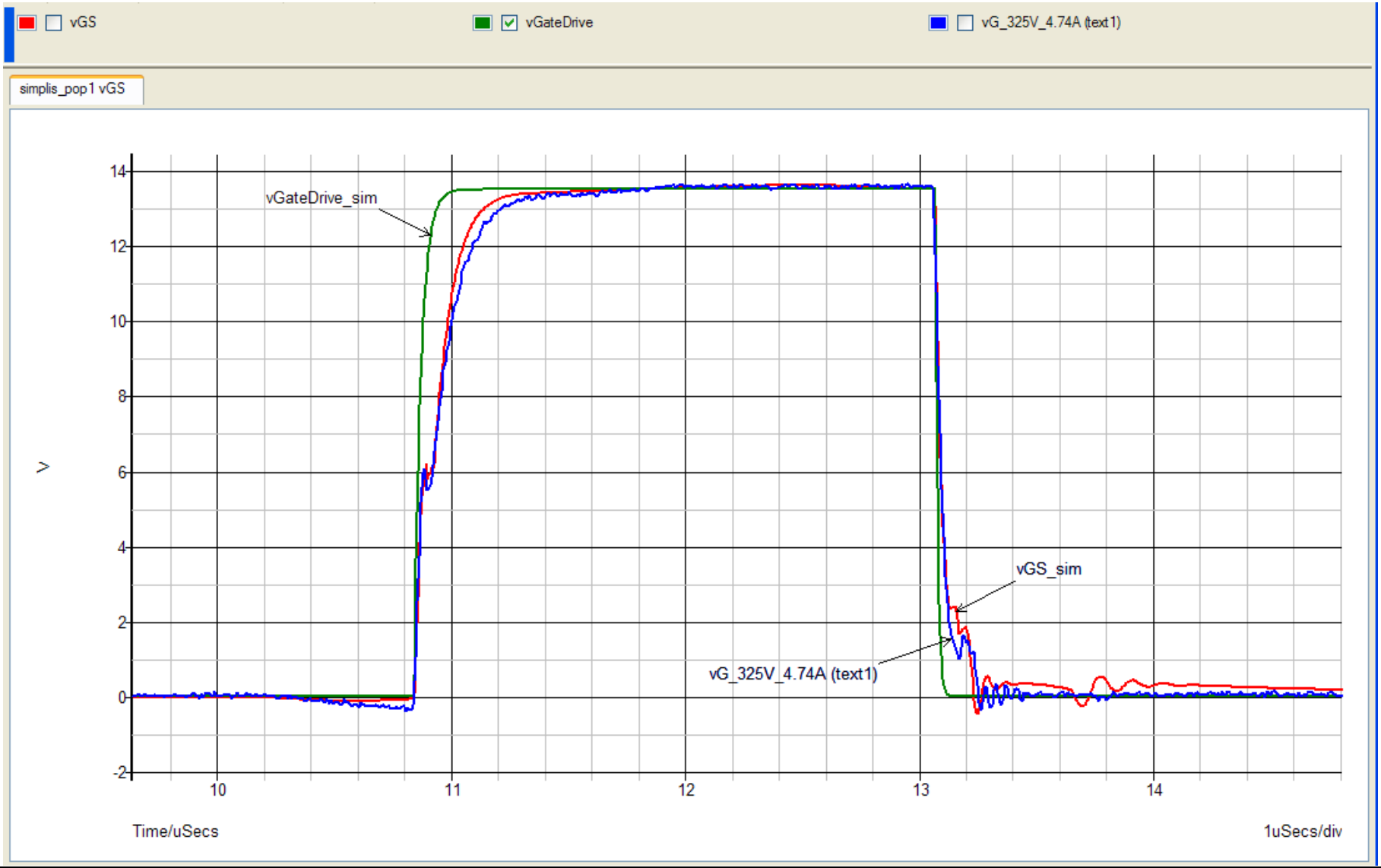
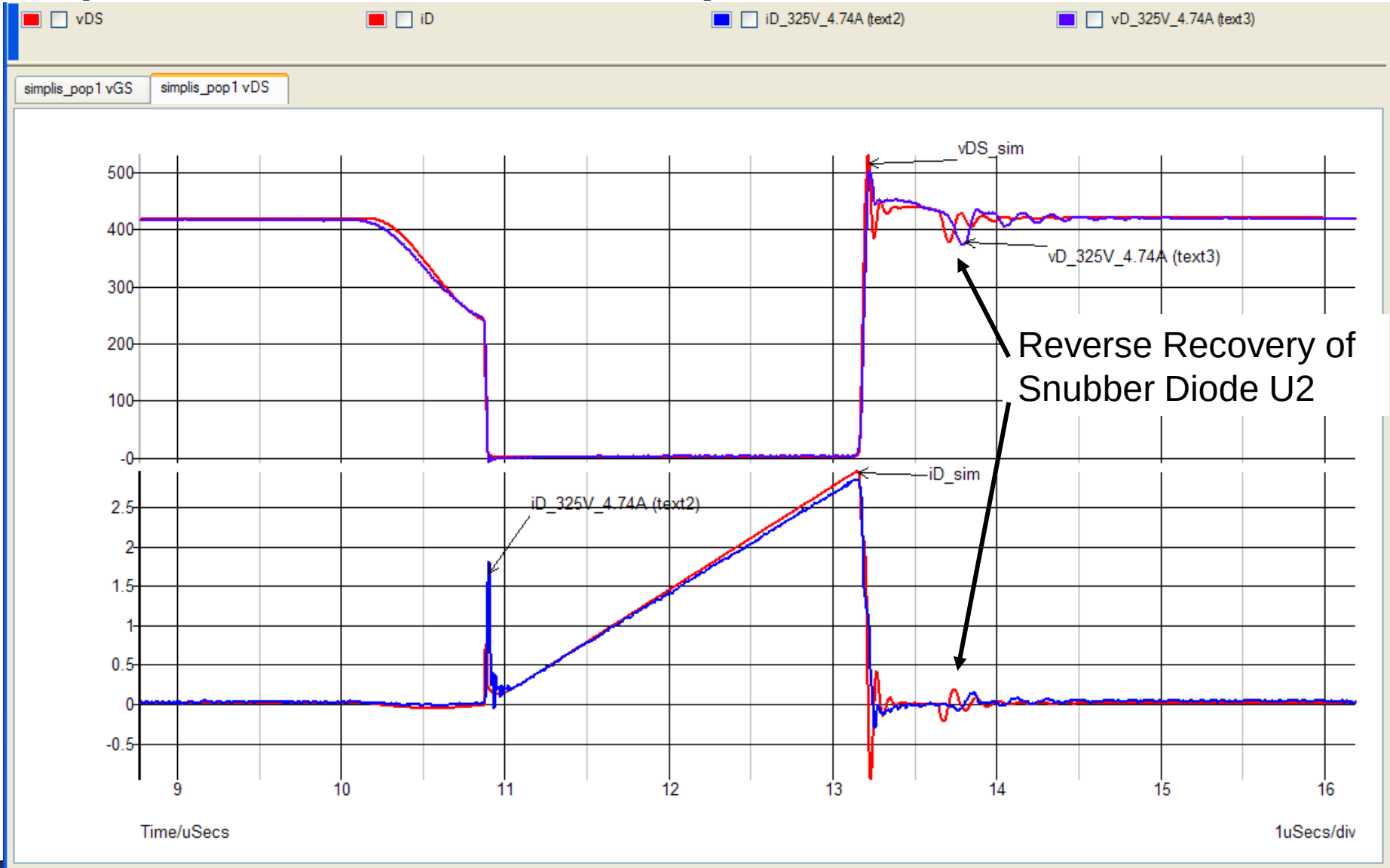
D.55.1

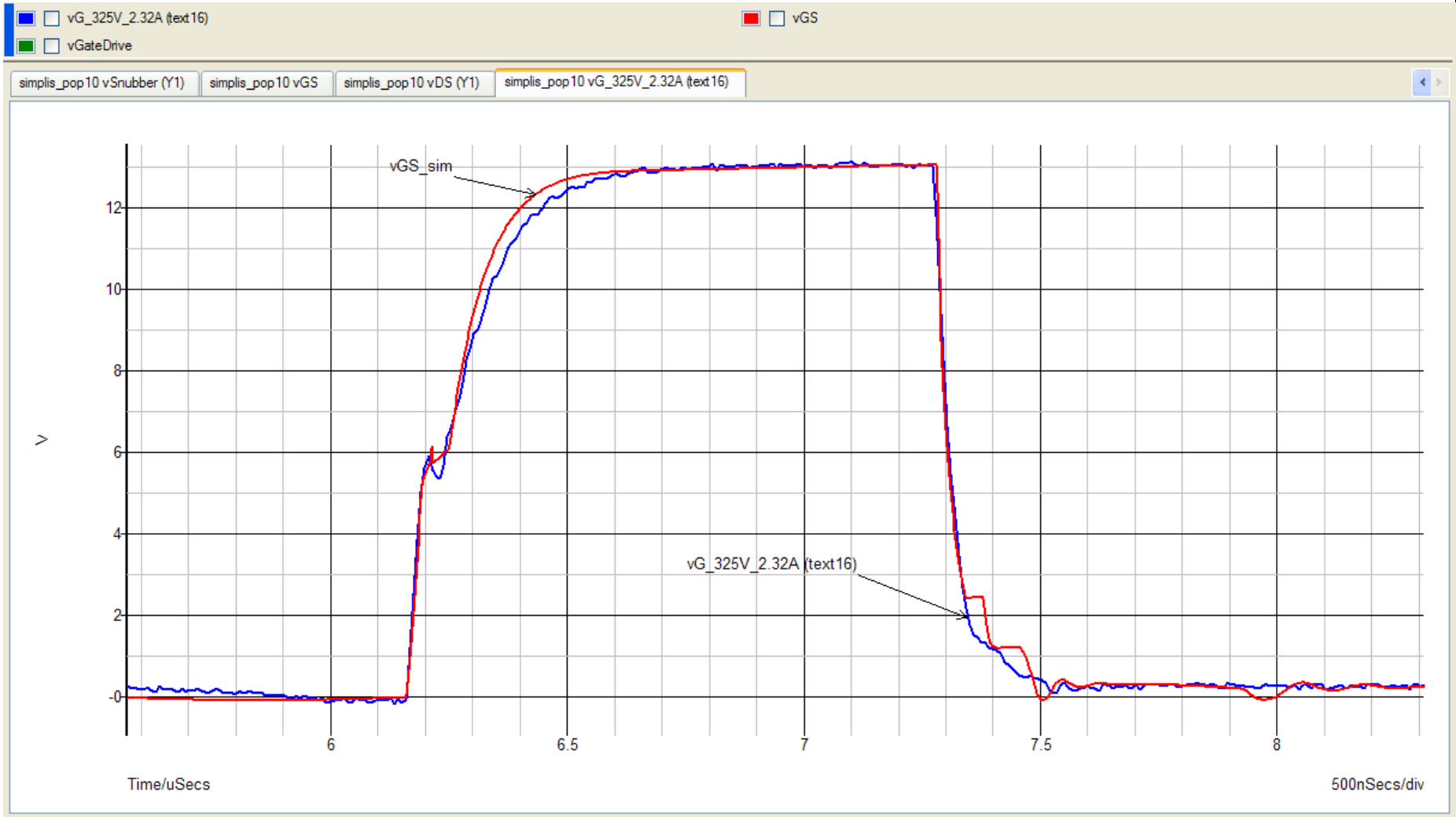
Gate Voltage v_{GS}
(Vin = 325V, Iout = 4.74A)



Drain Voltage v_{DS} and Drain Current i_D (Vin = 325V, Iout = 4.74A)

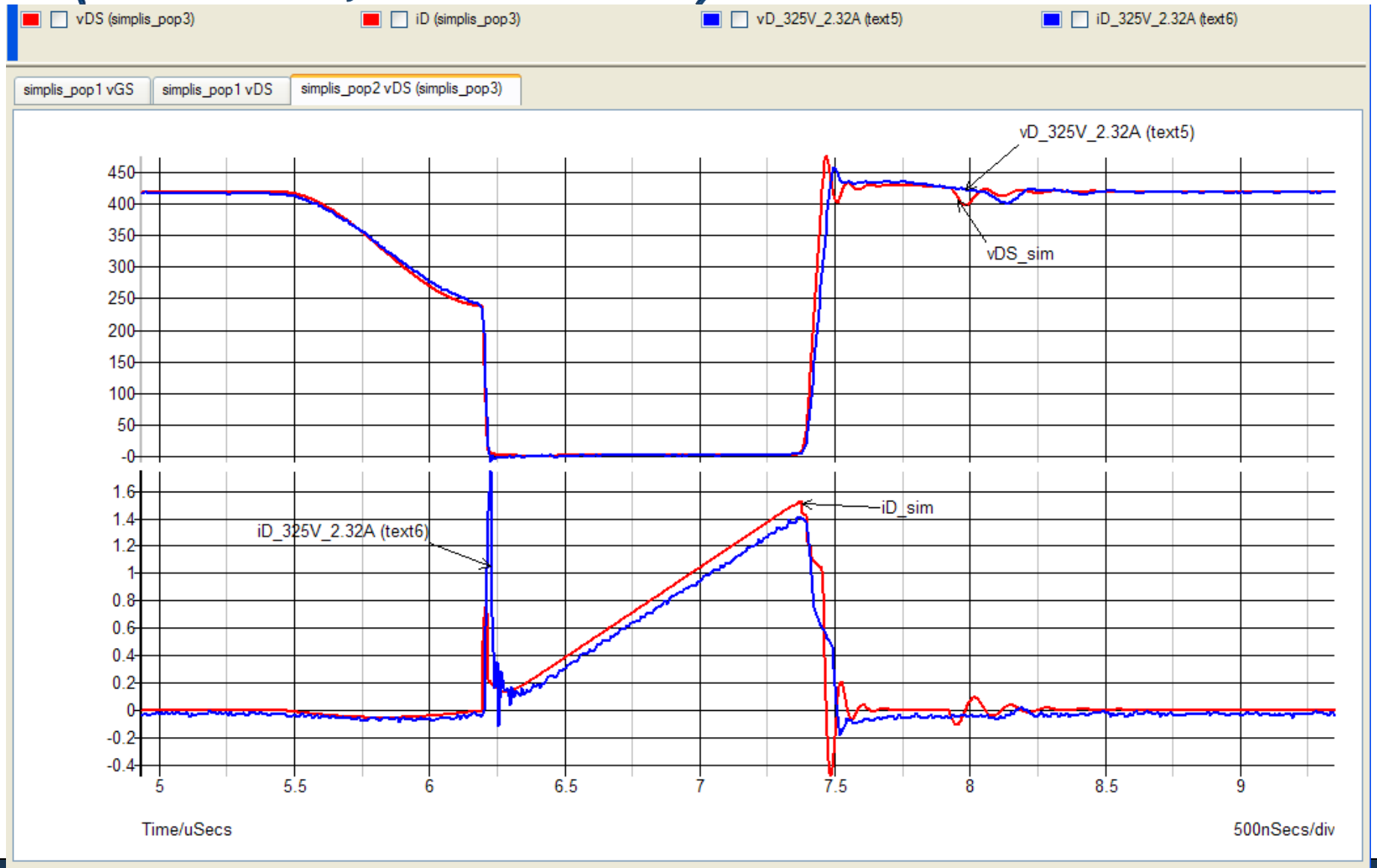


Gate Voltage v_{GS} (Vin = 325V, Iout = 2.32A)

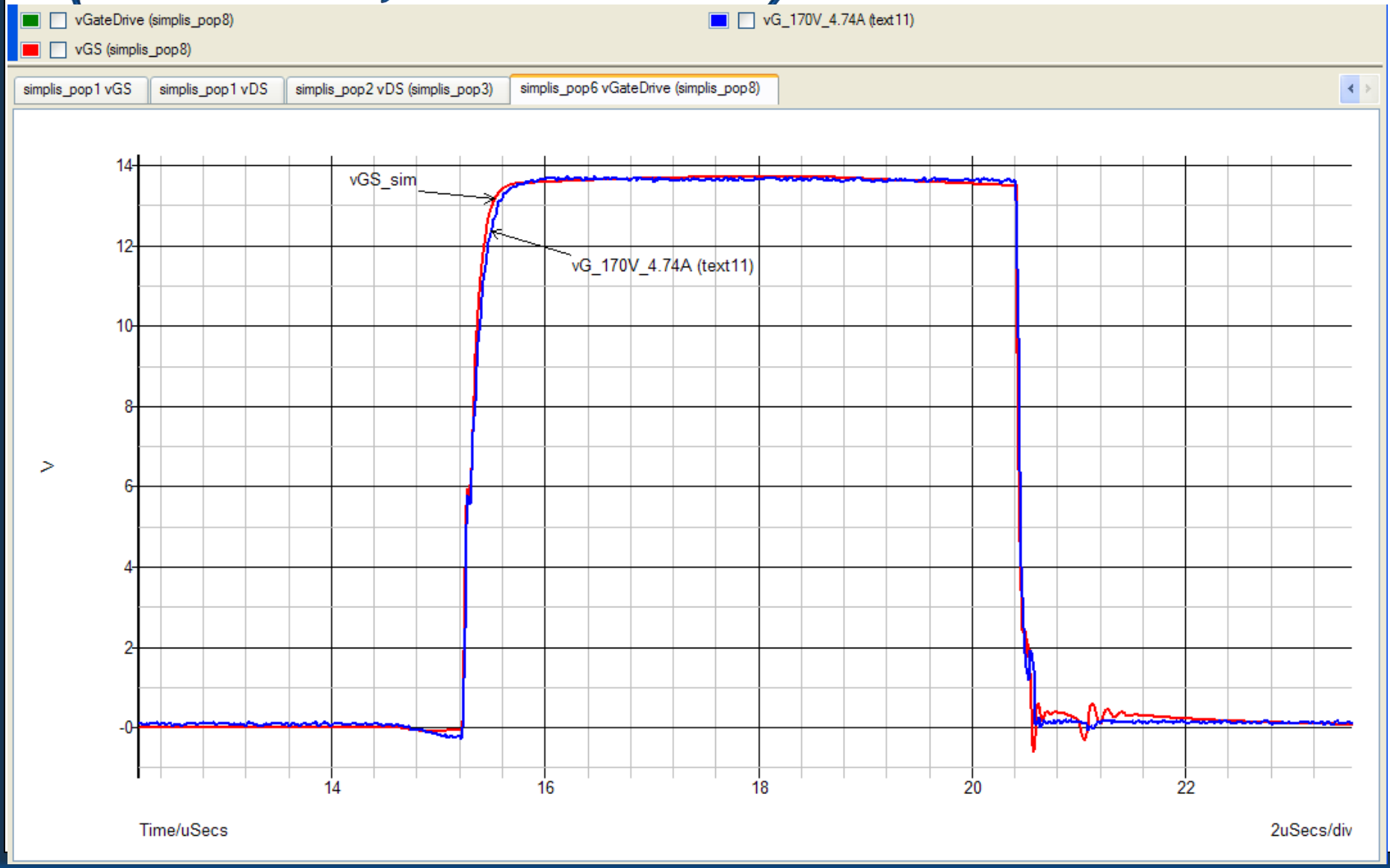


SIMPLIS TECHNOLOGIES

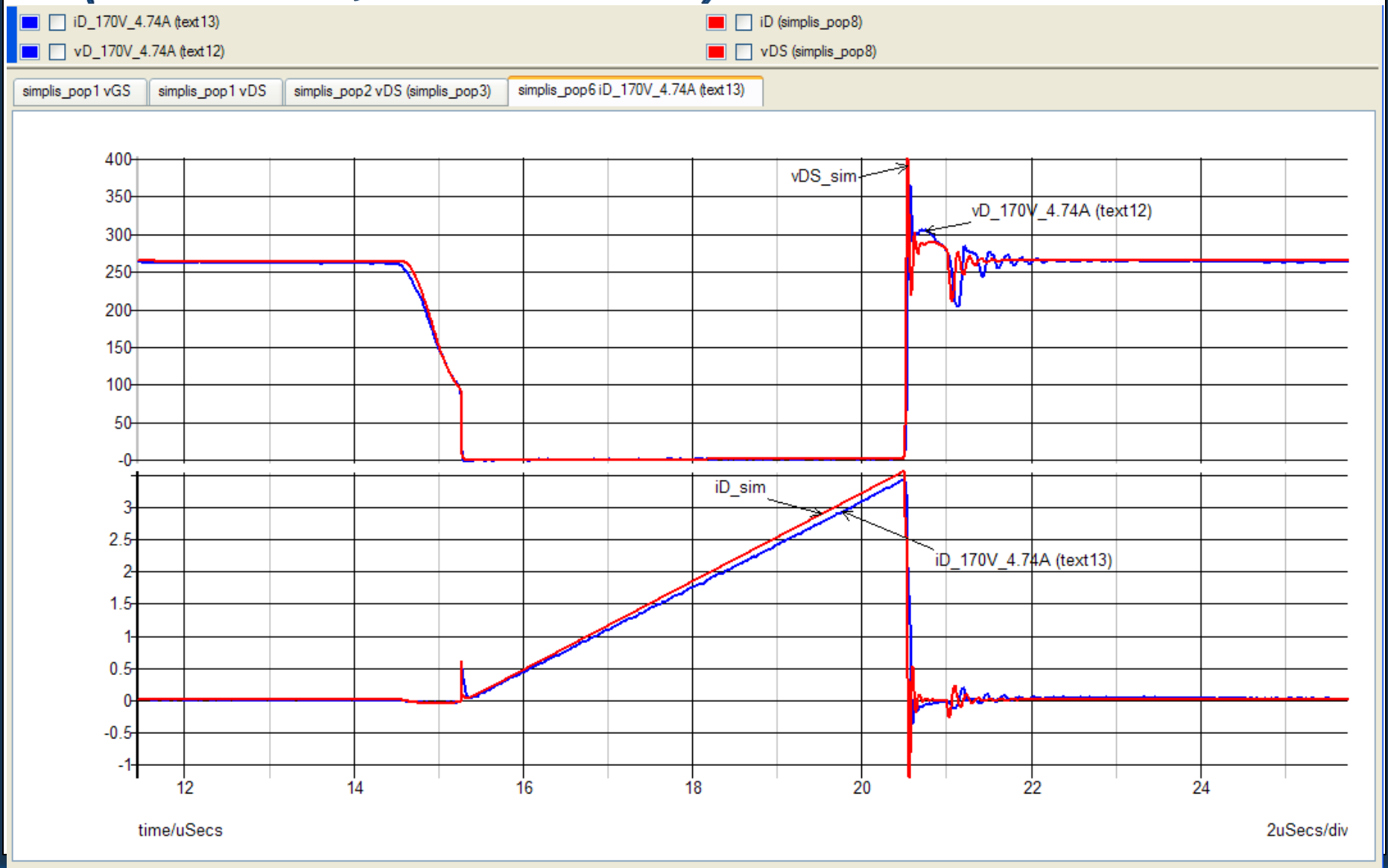
Drain Voltage v_{DS} and Drain Current i_D (Vin = 325V, Iout = 2.32A)



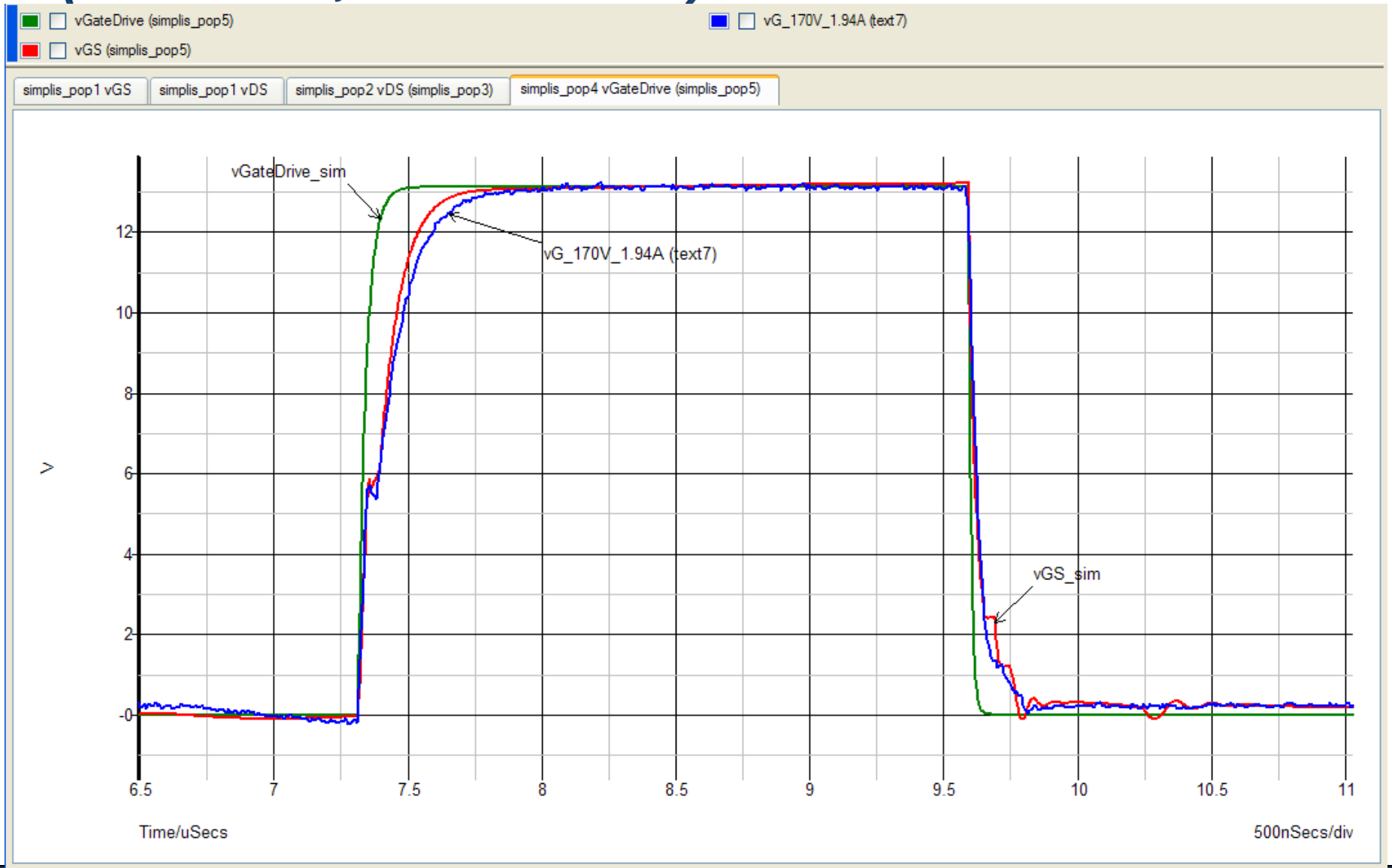
Gate Voltage v_{GS} (Vin = 170V, Iout = 4.74A)



Drain Voltage v_{DS} and Drain Current i_D (Vin = 170V, Iout = 4.74A)



Gate Voltage v_{GS} (Vin = 170V, Iout = 1.94A)



Drain Voltage v_{DS} and Drain Current i_D (Vin = 170V, Iout = 1.94A)

Switching Losses (1)

- Can get very good matching between simulated and measured waveforms
  - We are capturing the important aspects of FET waveforms pretty well
  - With reasonable measurements of silicon device parasitics
  - With reasonable estimates of
    - layout parasitics
    - magnetic device parasitics

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Switching Losses (2)

- Challenging to get sufficiently accurate ***measurements*** of vDS and iD to measure switching losses directly
- Would like better models for reverse recovery
  - First need better characterization data for devices
- Unknown layout parasitic can be estimated if have experience with similar packaging

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Switching Losses (3)

Having said all that

- Simulation can do a better and faster job than most hand analysis of estimating:
  - Switching losses before first hardware build
  - Sensitivity of losses to various layout and device parasitics

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Virtual Prototyping of Power Supply Designs

- Seminar Objective:
  - Show how new Design Verification Module (DVM) can be used to support Virtual Prototyping process
  - Show how DVM can be used to simulate switch and core losses
  - Digital Control Simulation

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Time is the most precious resource (1)

- Speed is essential to test for all “known” electrical design errors in a reasonable time
- You won’t find design errors that you don’t look for
- A comprehensive Test Plan includes hundreds of simulation tests.
- Want to invest simulation time where it will do the most good
- Need a clear and focused Test Plan that executes your Simulation Strategy

SIMPLIS TECHNOLOGIES

Time is the most precious resource (2)

- As Virtual Prototyping becomes more critical in the power electronics design process
  - Number of simulations becomes very large
  - For every simulation:

    Significant time required for:

    - Mechanics of set up and launching of tests
    - Managing, analyzing and archiving results

SIMPLIS TECHNOLOGIES

SIMetrix/SIMPLIS
Design Verification Module (DVM)

- DVM developed to support Virtual Prototyping process
  - Easy to use
    - Fast to set up
    - Flexible with User-defined Testplans
    - GUI to support test selection
  - Saves time by automating
    - Schematic preparation for each test
    - Management of simulation test suite
    - Report generation for simulation results

SIMPLIS TECHNOLOGIES

SIMetrix/SIMPLIS DVM

- Easy to use
  - ~ 5 min to set up schematic for DVM
  - New ***PowerAssist*** features
    - Make it easy for users to create own Testplans
    - Testplans defined by tab-separated ASCII text file
  - New, flexible GUI allows easy and more granular selection of tests

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DVM Test Reports (1)

- DVM Report Summary
  - Summary of number of tests
    - run, passed, failed, run with warnings, skipped
  - Links to individual test results
  - Links to Schematic, Testplan, machine readable results

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DVM Test Reports (2)

- Individual DVM Test Reports
  - Highlight featured waveforms
  - Perform measurements on specified waveforms
  - Compare results with specifications
  - Link to all probed waveforms for in-depth review
- Great for documenting design performance
  - Electronic assisted design reviews
  - Archiving of completed designs

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DVM - New Features

- Supports SIMetrix as well as SIMPLIS simulator
- ***PowerAssist*** – for Power Electronics users
- User-defined Testplans
- Supports multiple inputs and outputs
- Change parameter values from Testplan
  - .VAR and .PARAM statements
  - Local and Global parameter values
- Change hierarchical schematic values from Testplan
- GUI to facilitate selection of tests to run
- Accepts user-defined sources and loads

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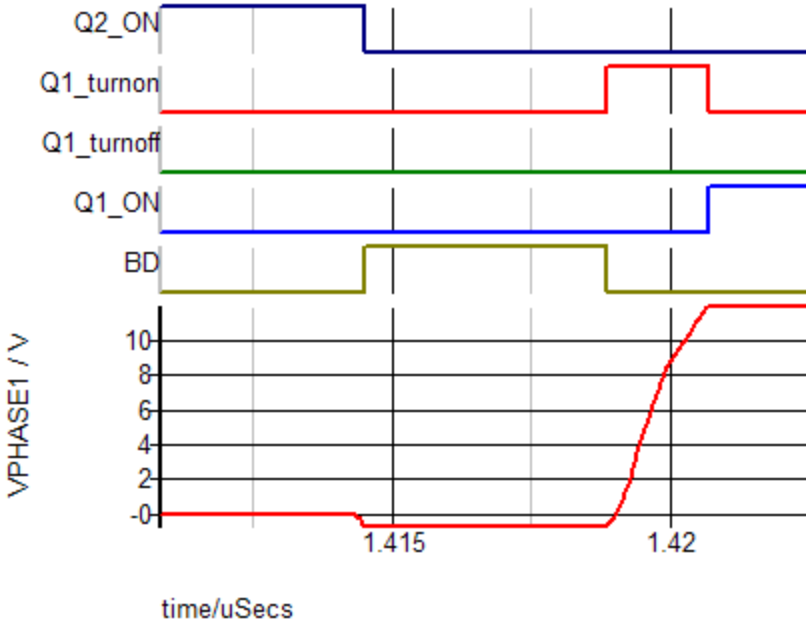
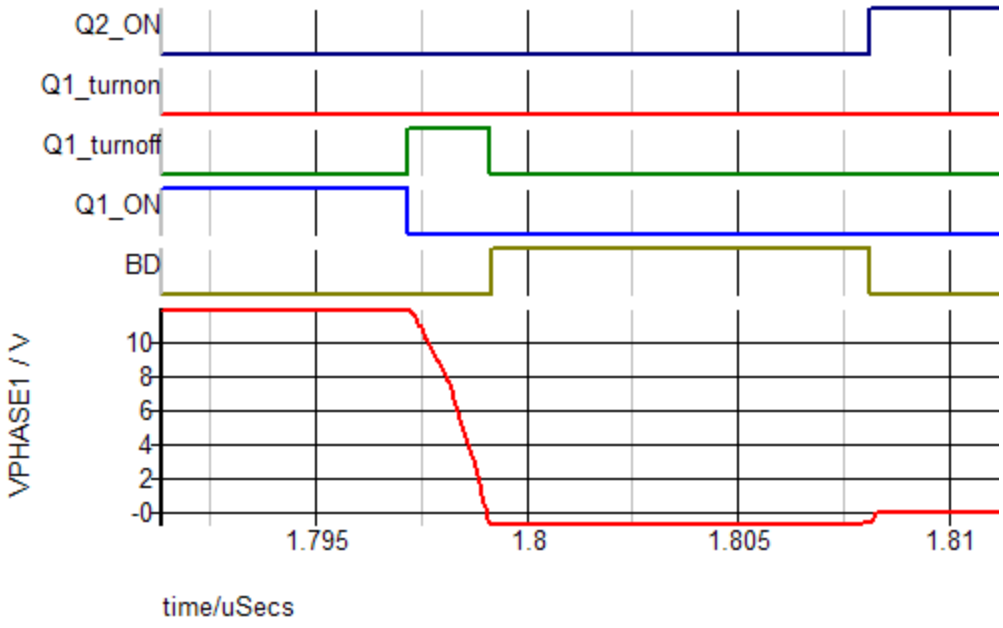
Sync Buck Switching Loss



High Side Q1 turn ON



High Side Q1 turn OFF

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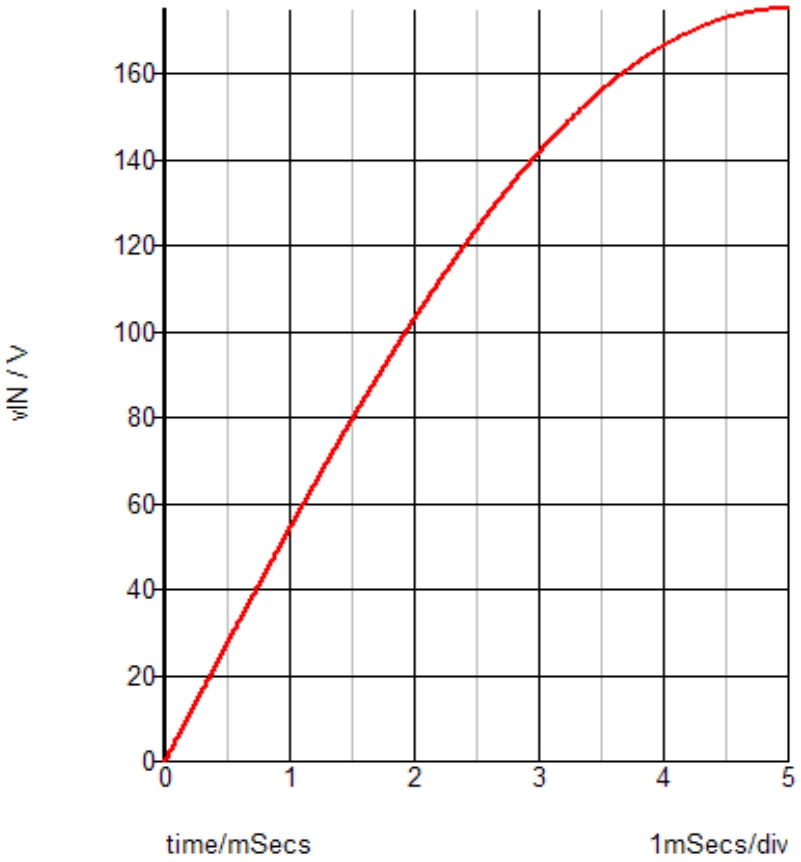
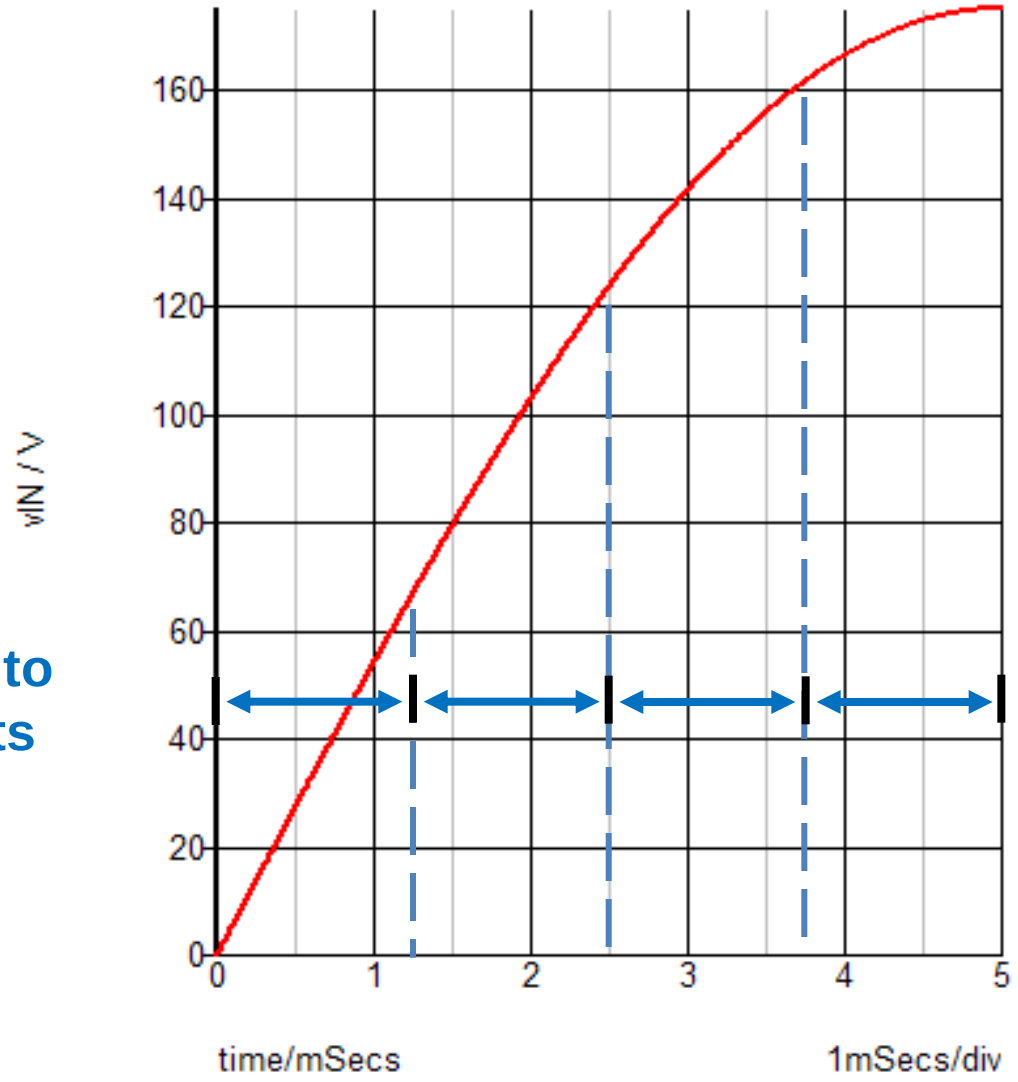
DVM – Measuring PFC Switch Loss

- Use Transient simulation to find AC steady state
- Then simulate ¼ sine wave
- But first…



DVM – Measuring PFC Switch Loss



Divide ¼ sine wave into N equal time segments

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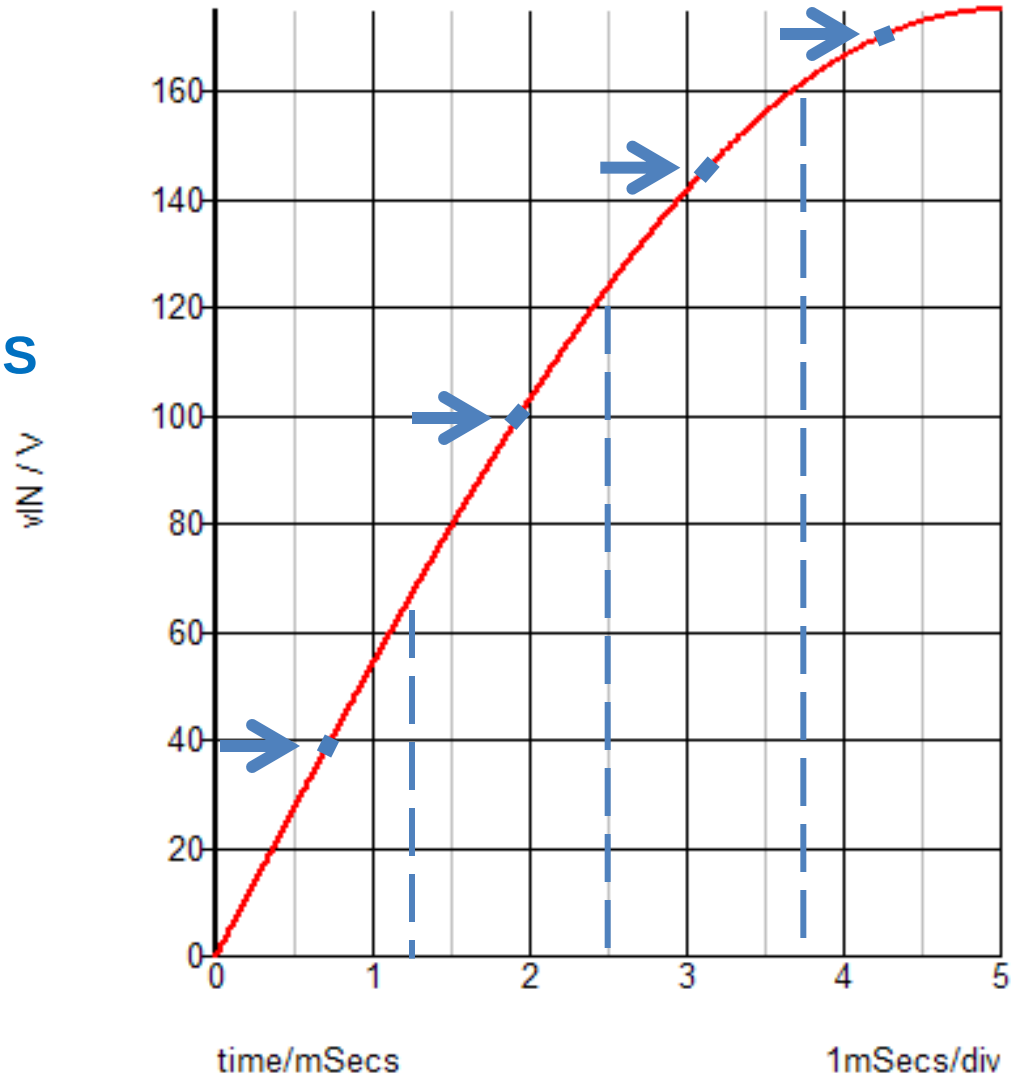
DVM – Measuring PFC Switch Loss

Then calculate the RMS voltage for each time segment



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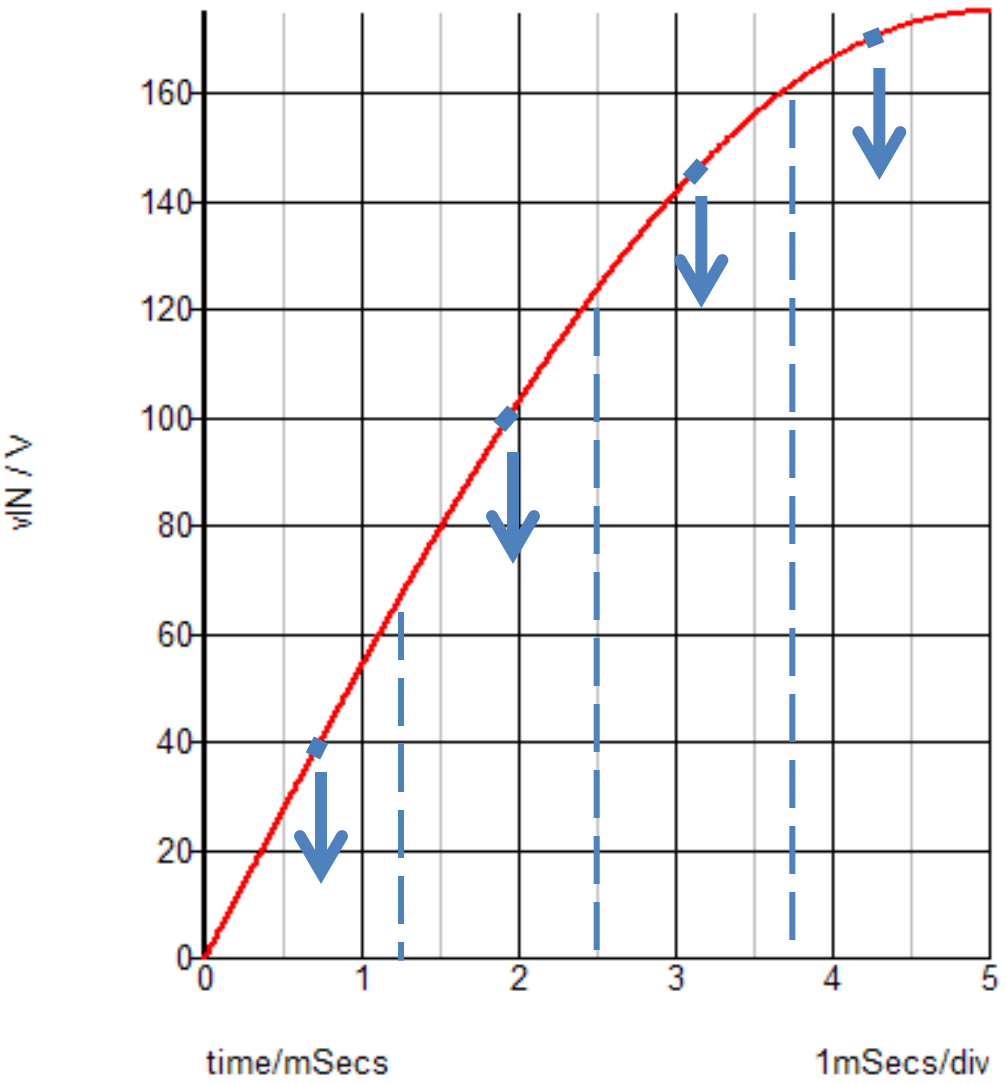
DVM – Measuring PFC Switch Loss

For each time segment find the time when the instantaneous input voltage equals value of RMS voltage



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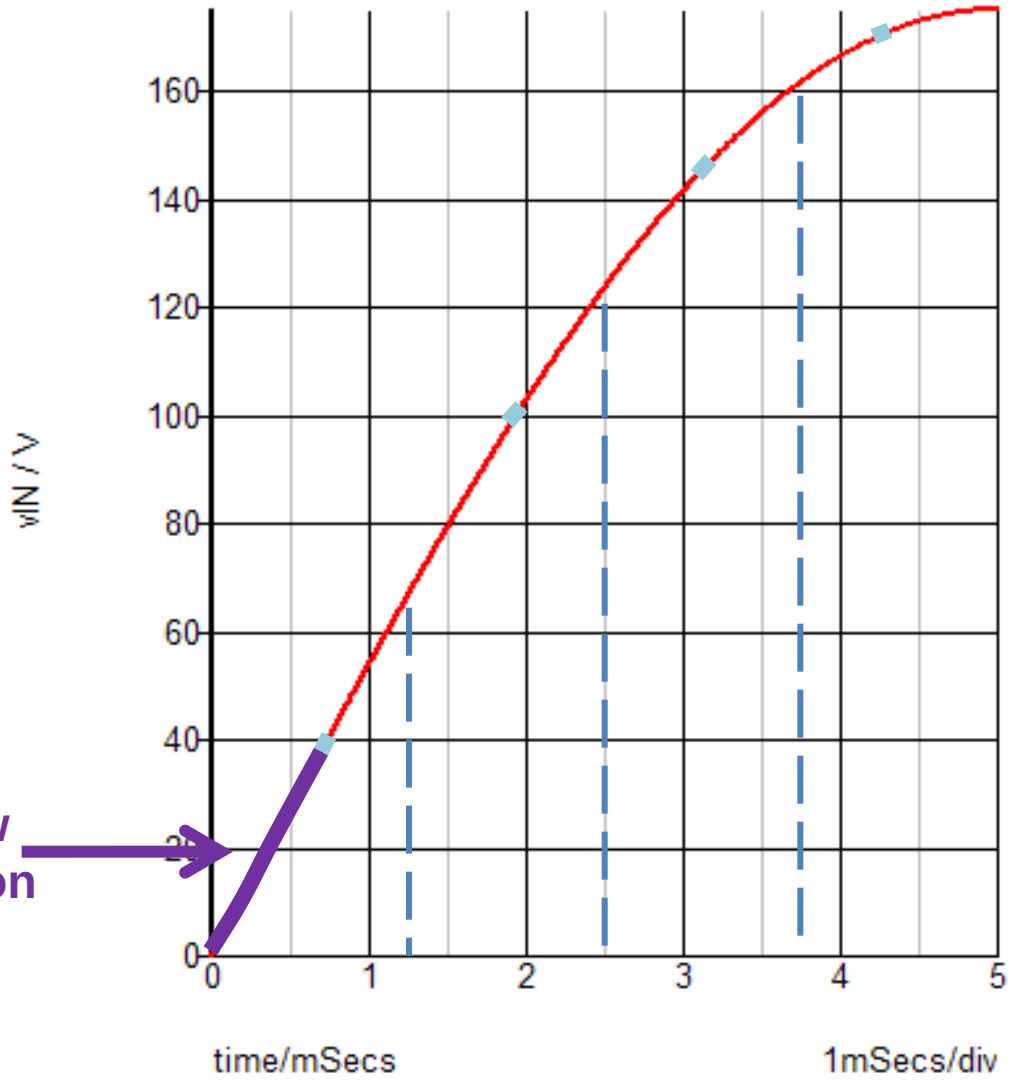
DVM – Measuring PFC Switch Loss

Daisy chain together simulation of ¼ sine wave of input voltage, beginning with

First time interval

Fast, Low Resolution

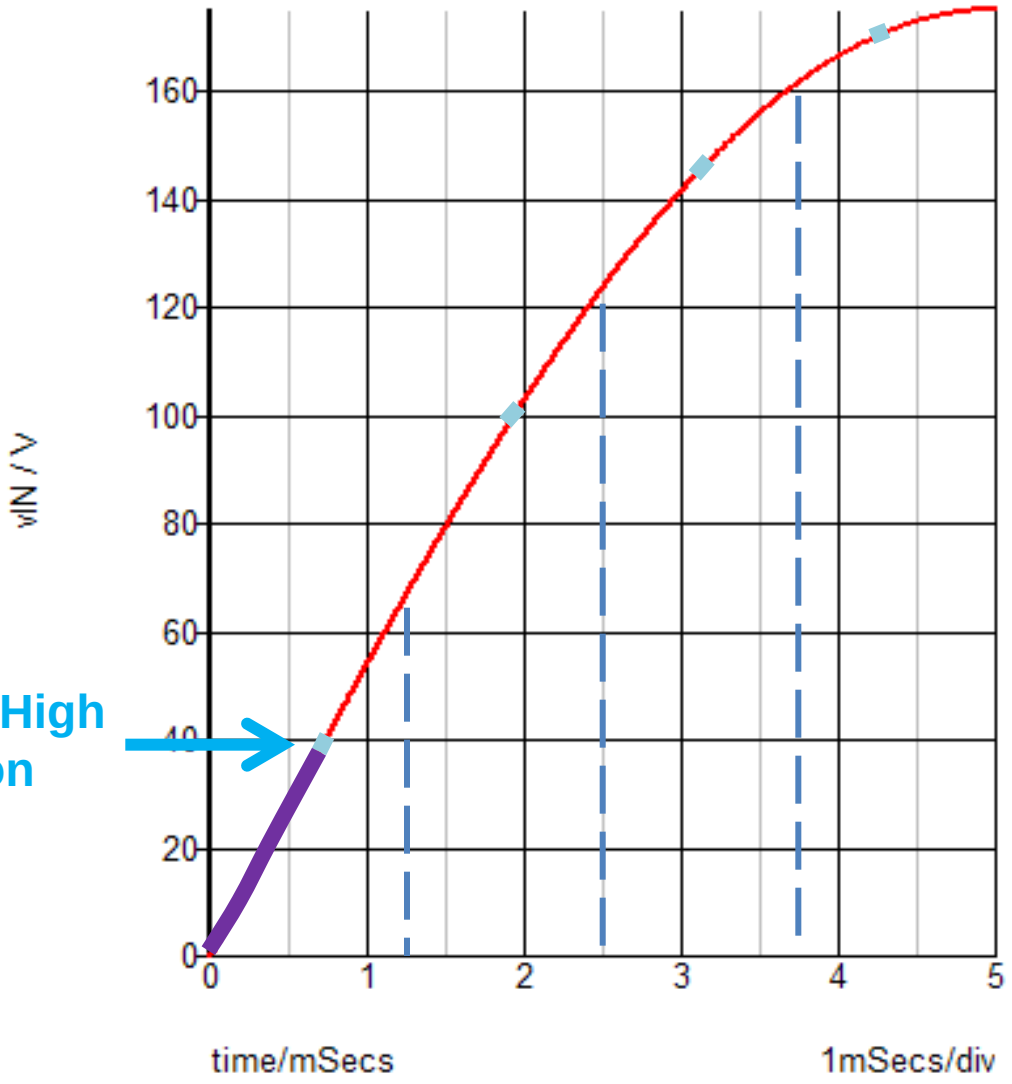


DVM – Measuring PFC Switch Loss

Daisy chain together simulation of ¼ sine wave of input voltage.

Followed by

3 cycles, High Resolution



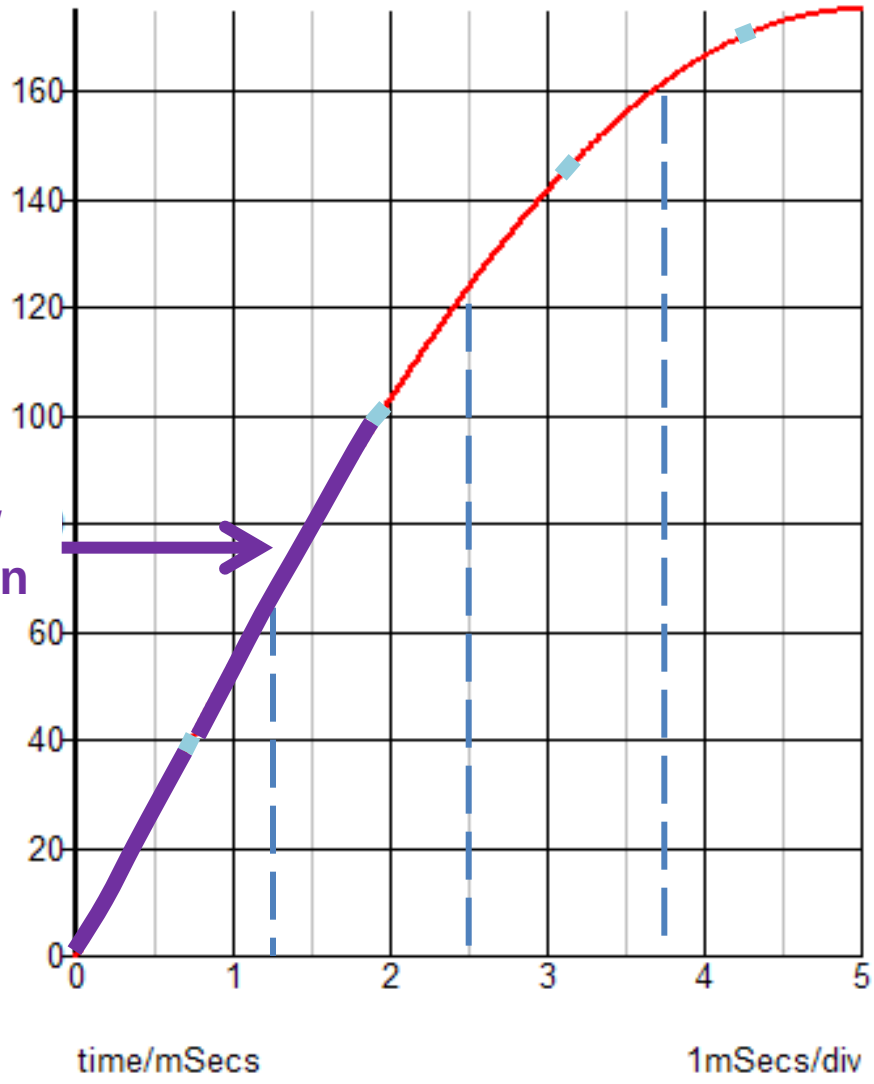
SIMPLIS TECHNOLOGIES

DVM – Measuring PFC Switch Loss

Daisy chain together simulation of ¼ sine wave of input voltage.

Then

Fast, Low Resolution



SIMPLIS TECHNOLOGIES

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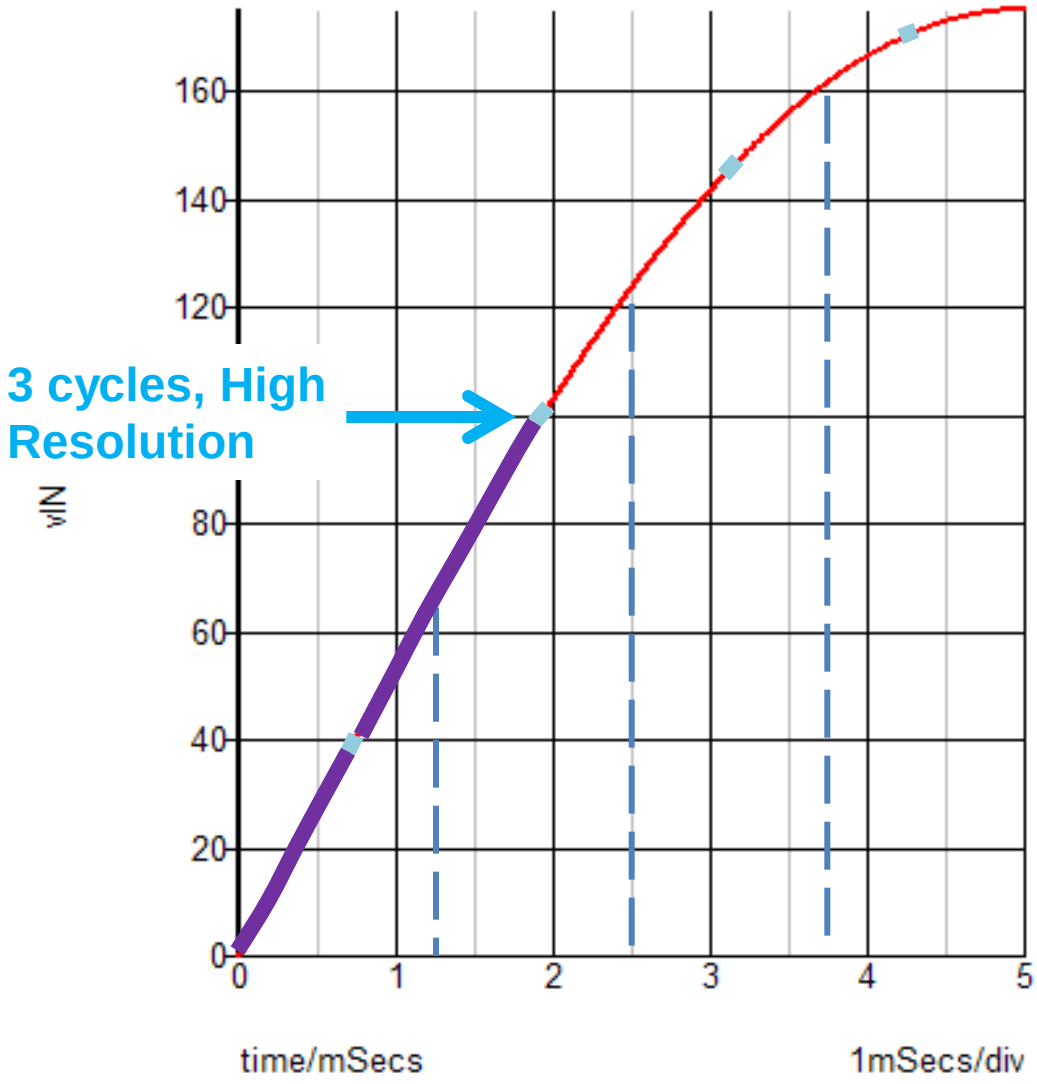

SIMPLIS TECHNOLOGIES

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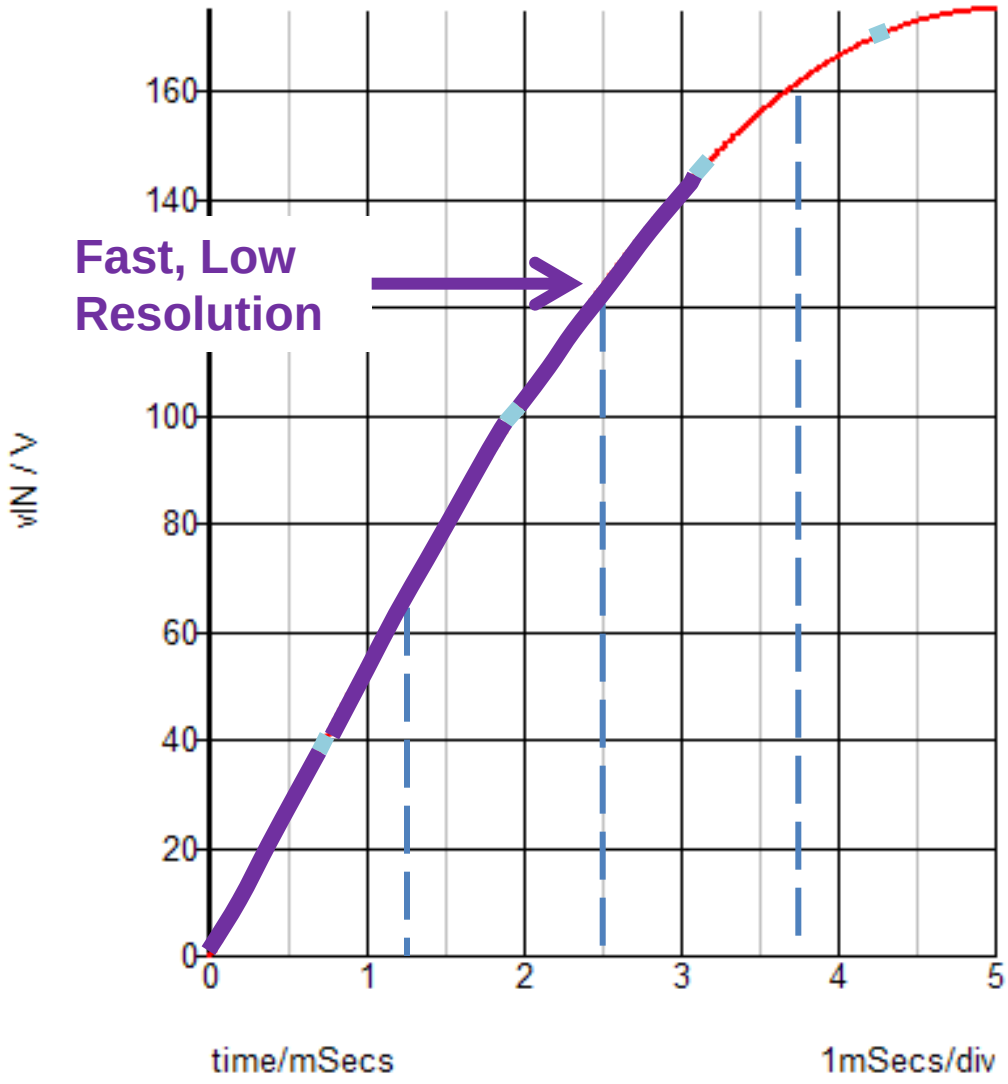

SIMPLIS TECHNOLOGIES

DVM – Measuring PFC Switch Loss

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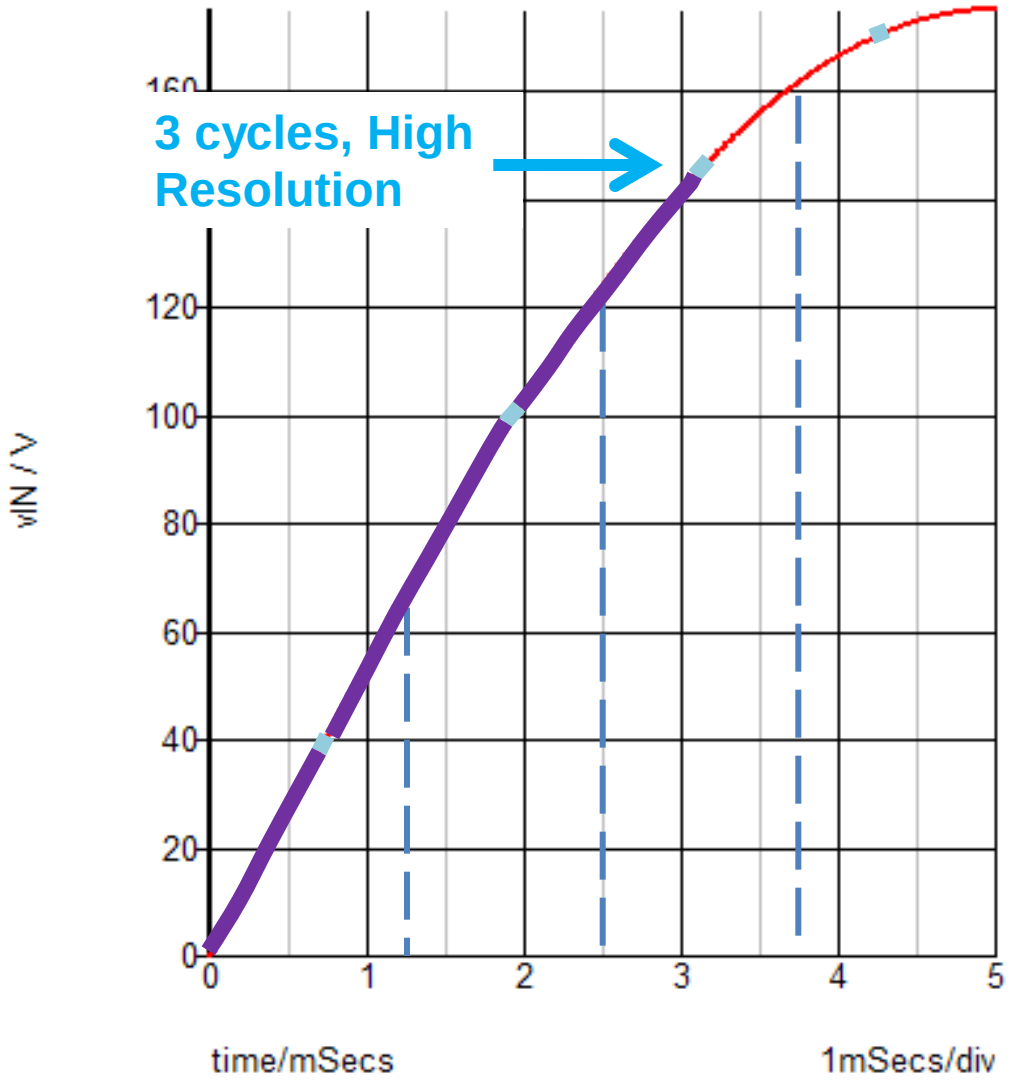

SIMPLIS TECHNOLOGIES

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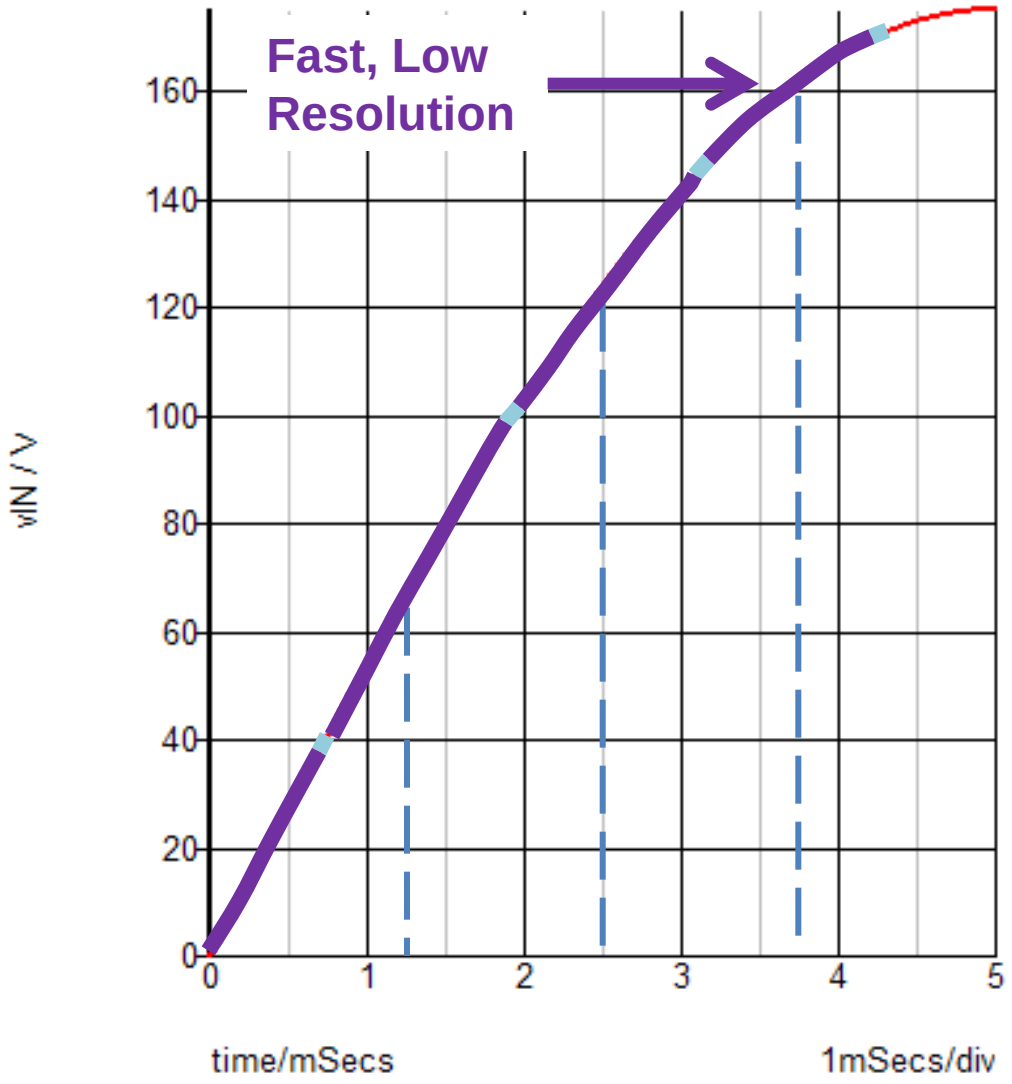

SIMPLIS TECHNOLOGIES

DVM – Measuring PFC Switch Loss

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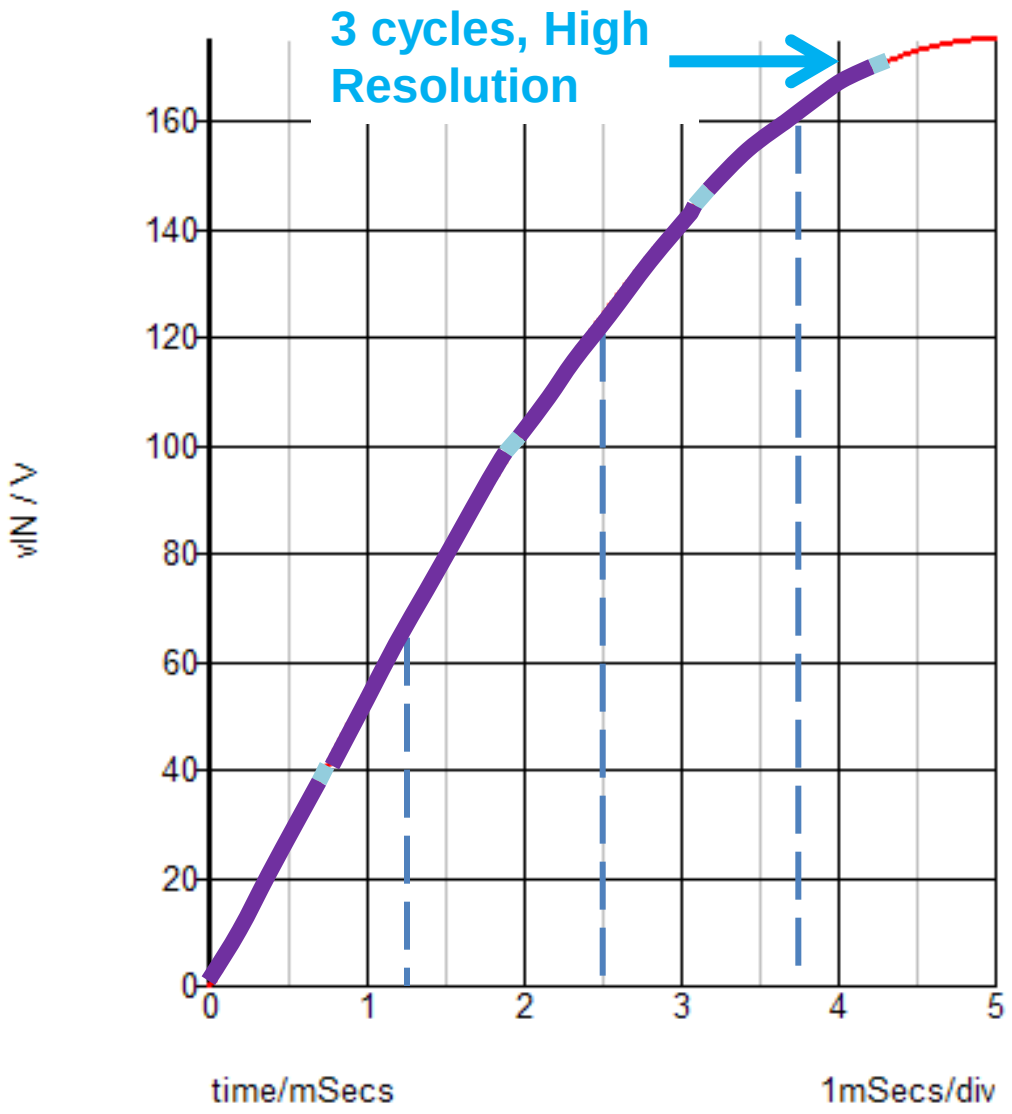

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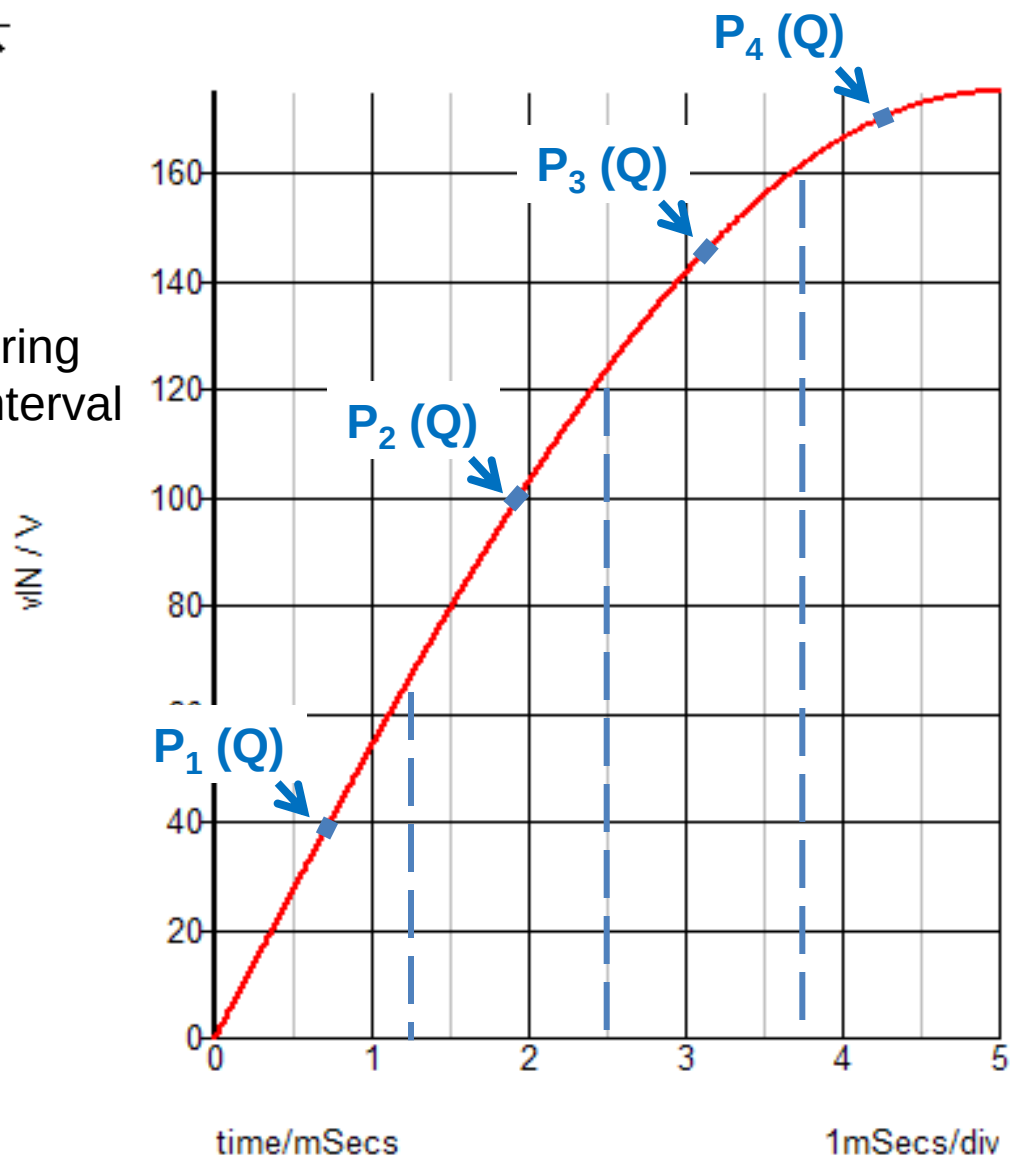
DVM – Measuring PFC Switch Loss

Measure the switch loss during each high resolution time interval

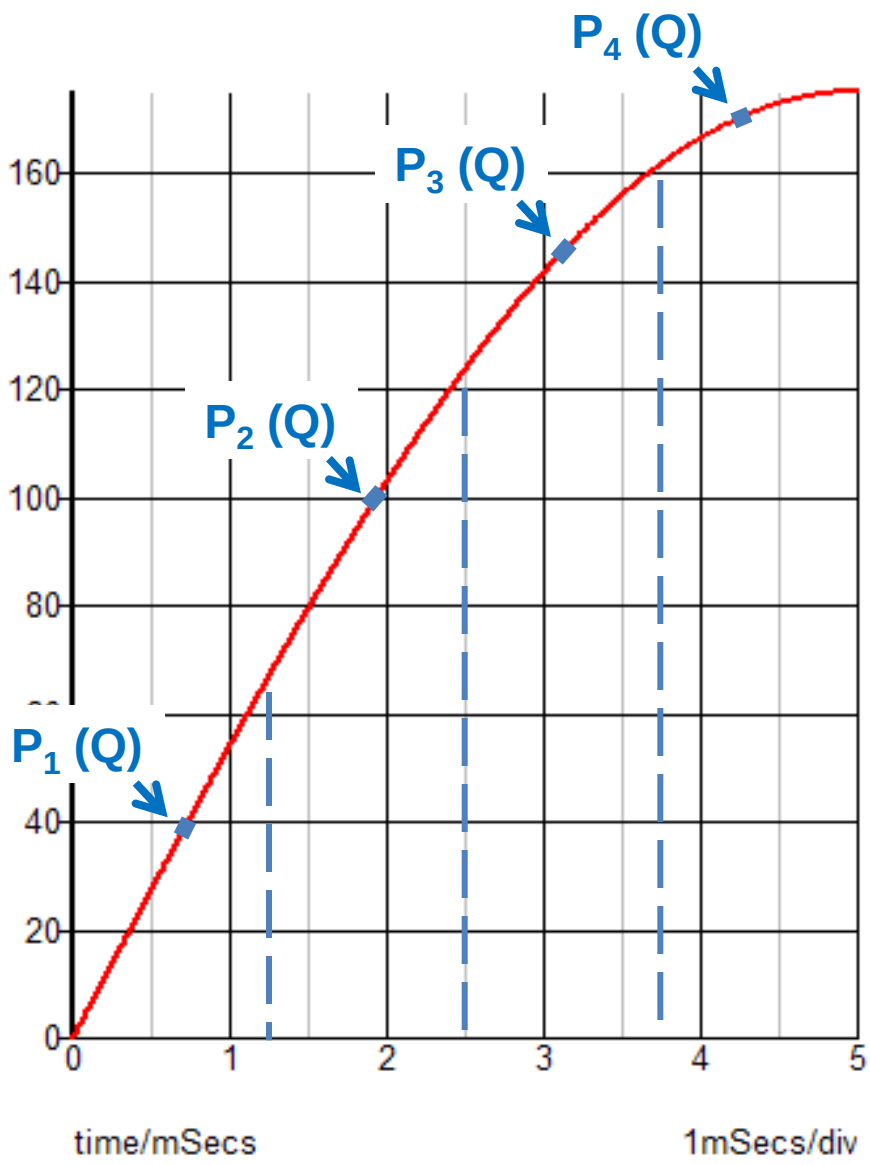


SIMPLIS TECHNOLOGIES

DVM – Measuring PFC Switch Loss

Finally, average these measurements for the total switch loss.

$$P(Q) = (P_1+P_2+P_3+ \ldots+P_N) / N$$



SIMPLIS TECHNOLOGIES

SIMetrix/SIMPLIS
Design Verification Module (DVM)

- Easy to use
  - Fast to set up
  - User-defined Testplans with ***PowerAssist***
  - GUI to support test selection
- Saves time by automating
  - Schematic preparation for each test
  - Management of simulation test suite
  - Report generation for simulation results

SIMPLIS TECHNOLOGIES

SIMetrix/SIMPLIS
Design Verification Module (DVM)

- Facilitates power supply performance characterization
- Detailed sensitivity and worst case studies
- Loss analysis
  - Sync Buck
  - Interleaved Boost PFC
- Reports summarize results and link to detailed waveforms

SIMPLIS TECHNOLOGIES

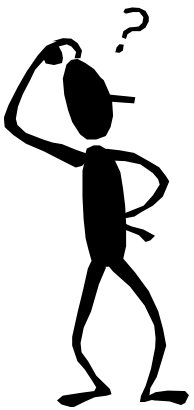
New Product Definition for Power Management ICs

- Significant Process Trend
  - Use of SIMPLIS PWL simulation behavioral model to define new products
  - Create behavioral models that describe all critical features
  - Thoroughly test PWL behavioral model of proposed new product in system application circuit
    - Over whole anticipated application space
    - Compare results with customer system specs

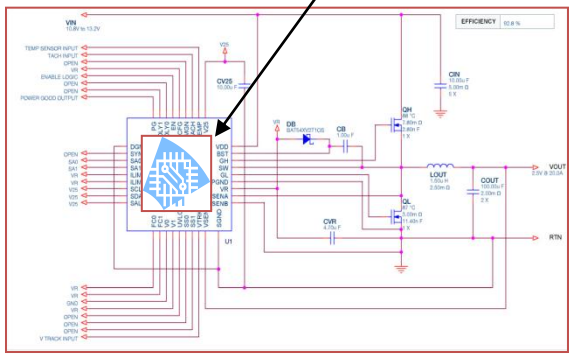
SIMPLIS TECHNOLOGIES

Traditionally

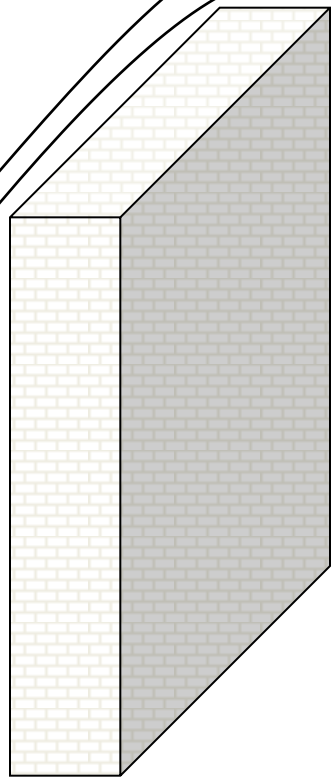
New Product Definition



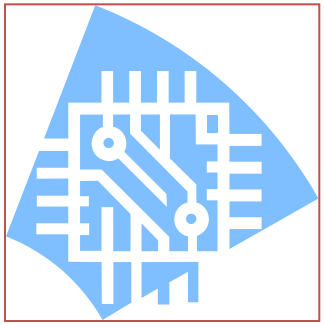
New Product Architect



Test & Verification



IC Designer



IC Design

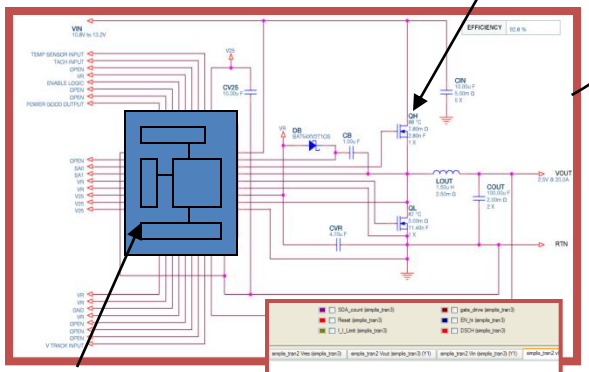
SIMPLIS TECHNOLOGIES

With SIMPLIS PWL Virtual Prototype

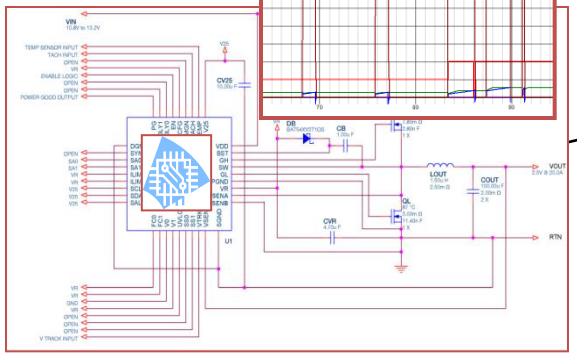
New Product Definition

New Product Architect

Application Schematic

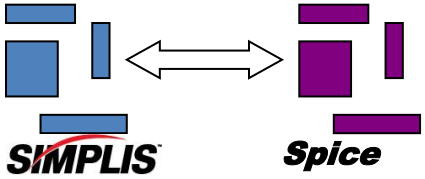


SIMPLIS IC Building blocks

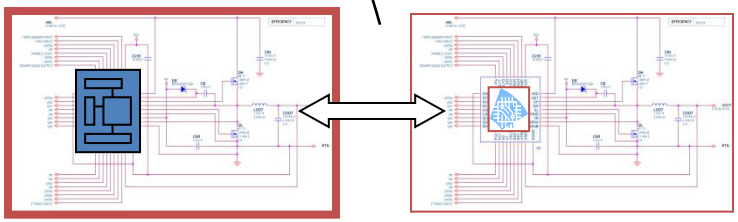


Test & Verification

IC Designer



IP Block Mapping



SIMPLIS TECHNOLOGIES

New Product Definition
SIMPLIS PWL Behavioral Models

- Provides much crisper new product definition between System Engineer and IC Circuit Designer
- New Product Definition includes:
  - Clear relationship between IC spec and system level performance
  - Clear definition of Top level IC architecture
  - Quantitative specs (delays, waveforms, rise/fall times, bandwidth) of each input/output for each major element in Block Diagram
  - Clear architecture of critical blocks

SIMPLIS TECHNOLOGIES

SIMPLIS -- Simulation of Digital Control

- Have already demonstrated very good accuracy and speed
- Detailed digital implementation
  - Captures sampling and delay behavior
  - Captures discretization error from finite number of bits
    - Hardware implementations
    - Firmware implementations
- Early concept design
  - Captures all sampling and delay
  - POP and AC analysis

SIMPLIS TECHNOLOGIES

Thank you!

Please contact Martin Chiou, You-Shang Tech. Corp.
Tel : 07-7104008, 0910878978

Download Circuits and Materials:

http://simplistechnologies.com/downloads/YouShang2011

SIMPLIS TECHNOLOGIES